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18 OCTOBER 2019

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Intel

Addressing 5G RF-FE Control Challenges with MIPI RFFE℠ v3.0

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Agenda

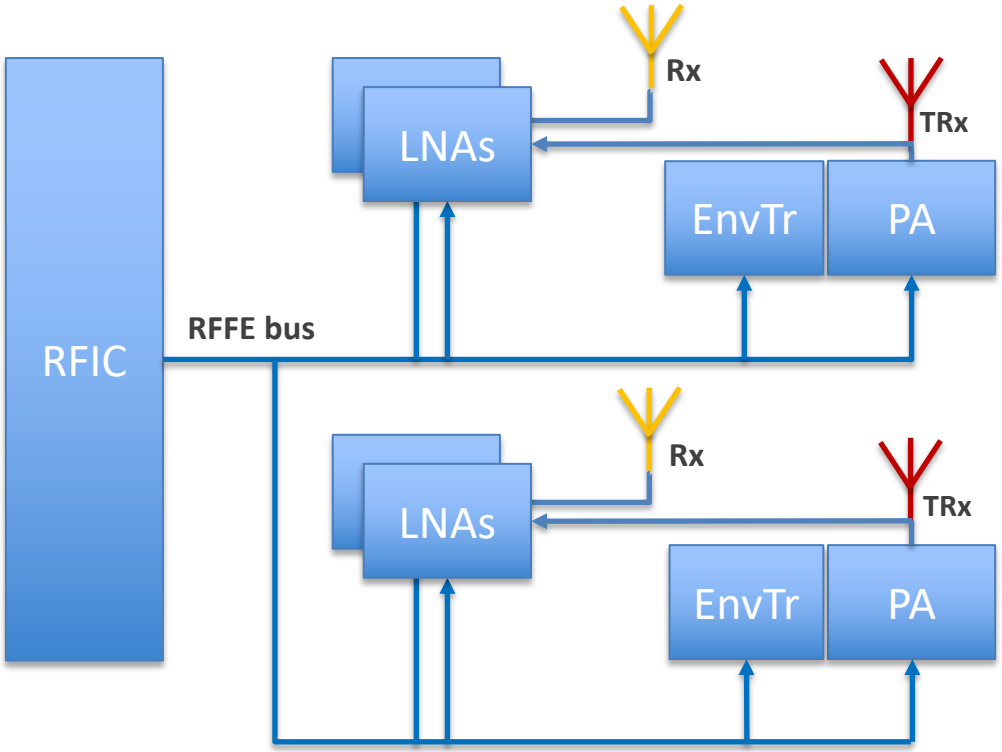
- Problem Statement
  - Abstract 5G sub 6 GHz RF Front End
  - Use case with tight Tx timing
  - Use case with tight Rx timing
- Solutions
  - Strategies to solve the trigger congestion problem
  - How to separate the trigger programming from the actual triggering
  - Revised use cases using timed triggers
- Timed Trigger Design Topics
  - Designing an RFFE master controller
  - Designing an RFFE slave controller

- Mappable Triggers (an additional feature)
- Questions

5G RF-FE Control

- Timing & Requirements

Abstract 5G Sub 6 GHz, RF Front End (RFFE)



Frequency Range 1 RFFE

- Receive
  - 4x4 DL MIMO
  - Inter-band Down Link Carrier Aggregation (DL CA)
- Transmit
  - 2x2 UL MIMO and/or
  - Inter-band Up Link Carrier Aggregation (UL CA)
  - PAs with Envelope Tracking (EnvTr)

RFFE Control Architecture

- Number of buses to be limited
  - ideally: 1
  - in reality: several

Command Sequences (CS) to various Front End components interfere!

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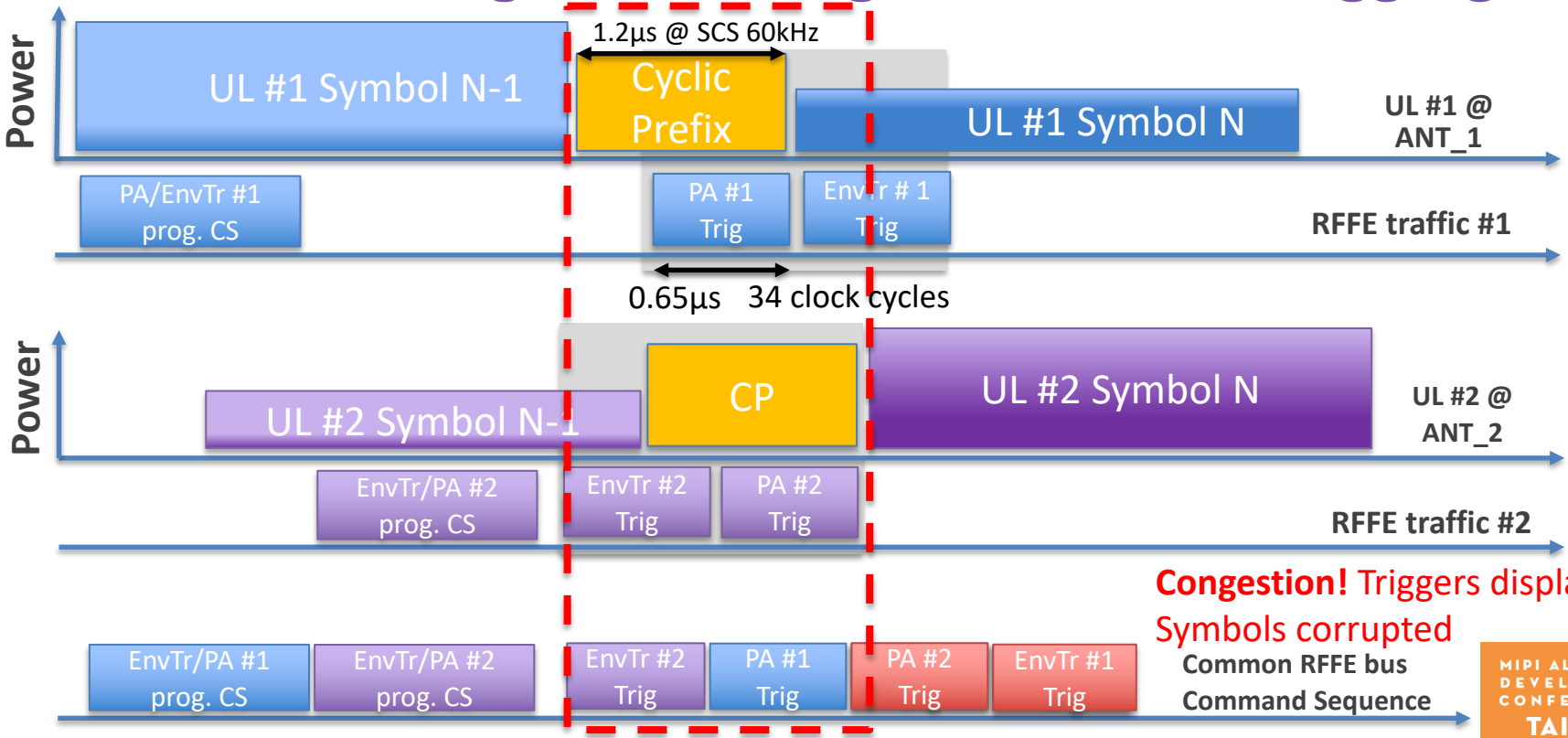
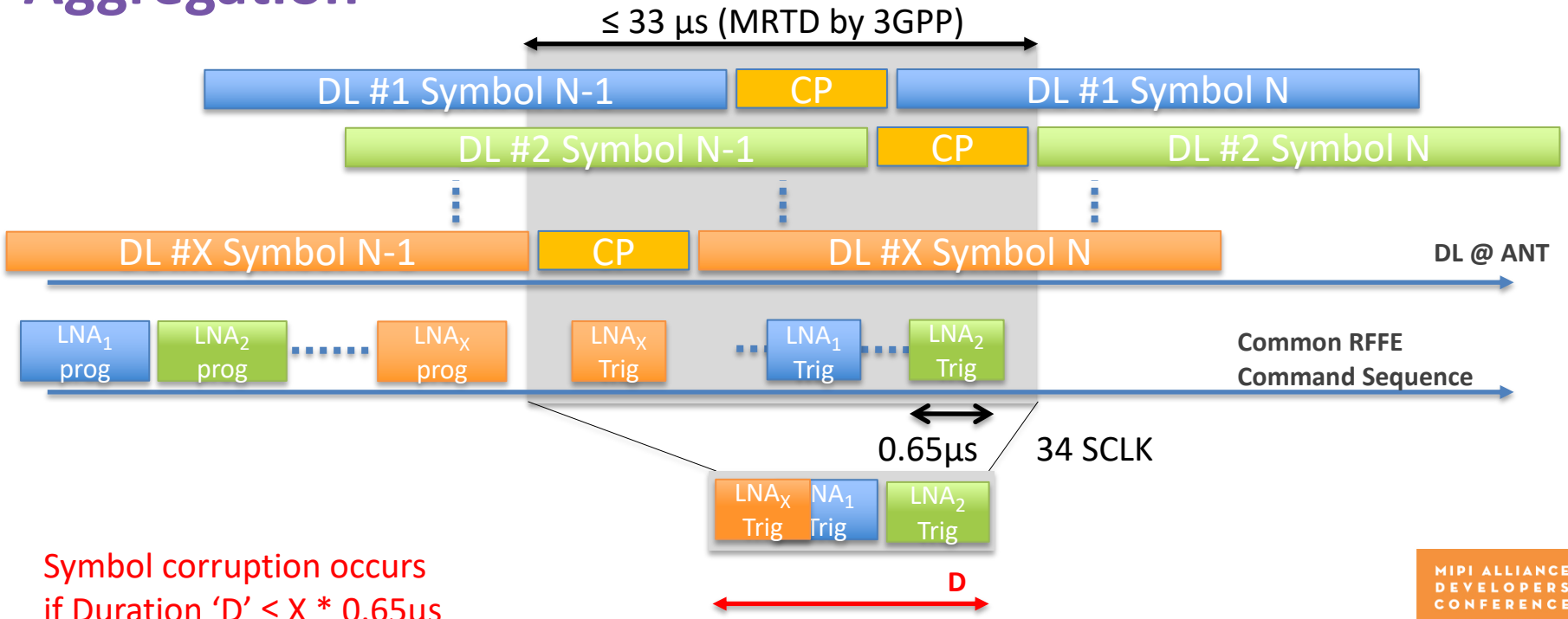
Use Case with Tight Tx Timing: 2*UL Carrier Aggregation



Use Case with Tight Rx Timing: X*DL Carrier Aggregation

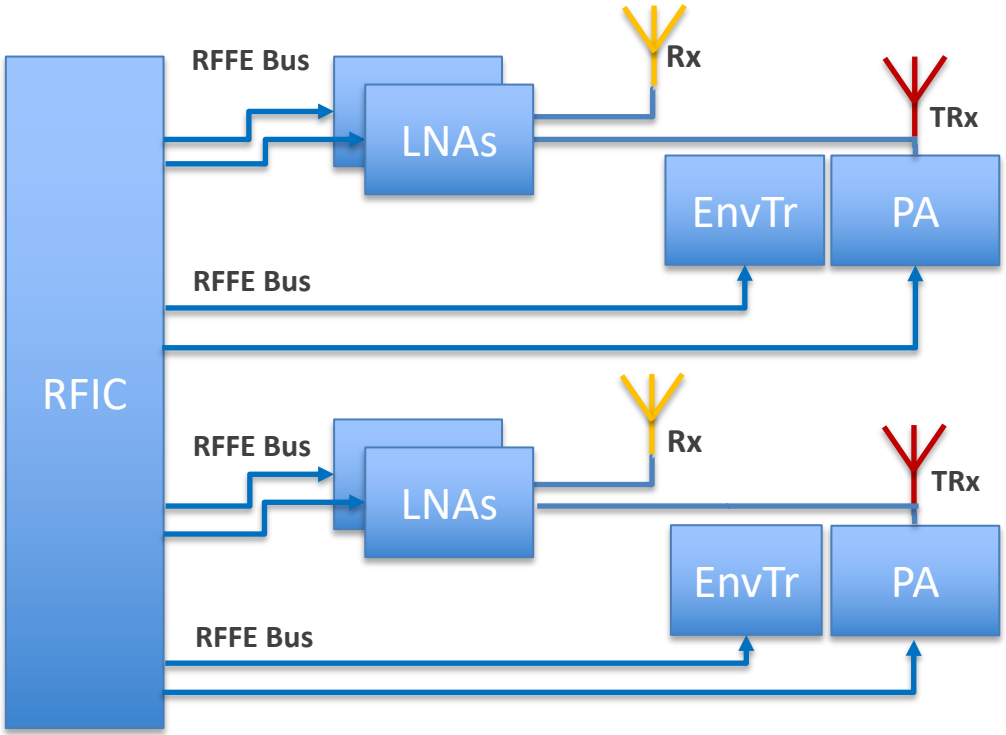


Symbol corruption occurs
if Duration 'D' ≤ X * 0.65µs

Potential Solution (Hardware)

- How to solve the RFFE bus congestion
- Duplicating resources

Duplicated RFFE Buses



Spatial Solution

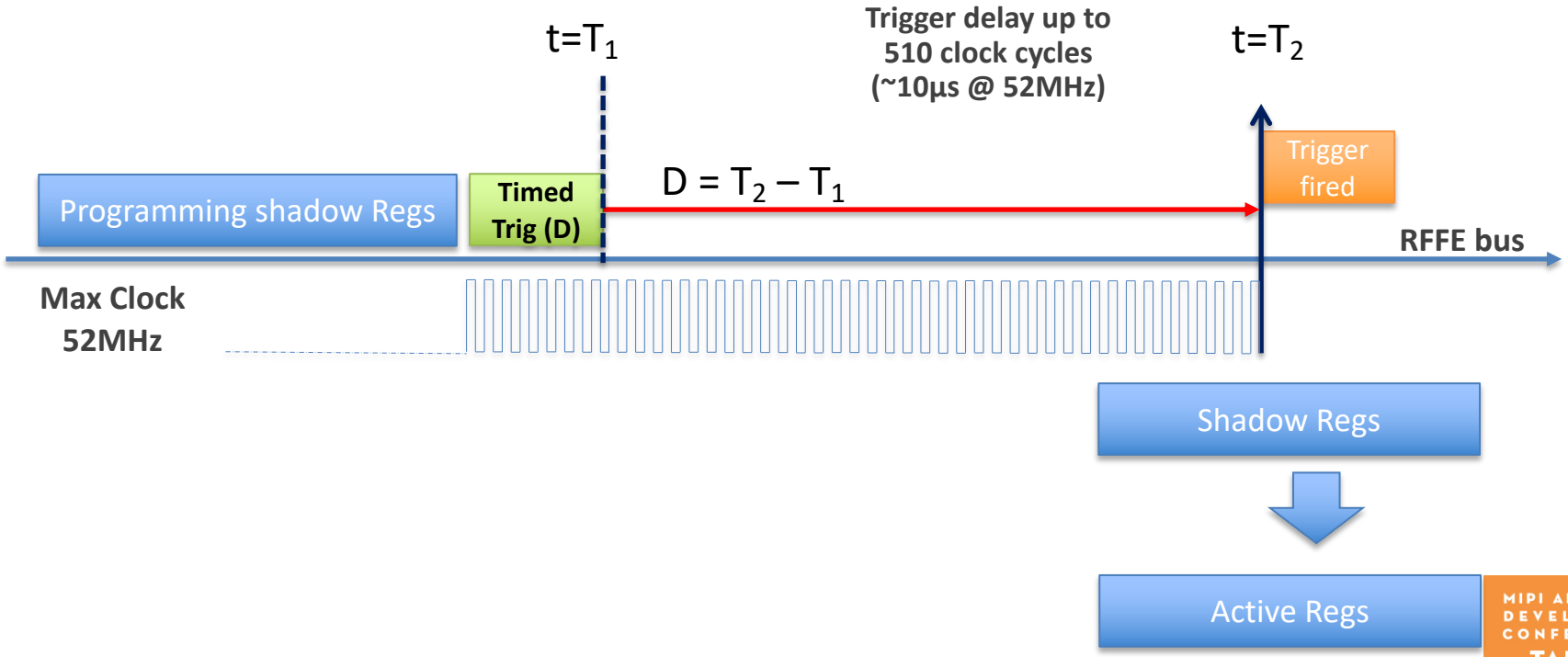
- Concurrently operated FE components shall not share a common bus
- Requires to know ALL use cases in advance
- Worst case: 1 bus per component
- Very costly in PCB area and routing

Not flexible for future requirements

Potential Solution (Programmable)

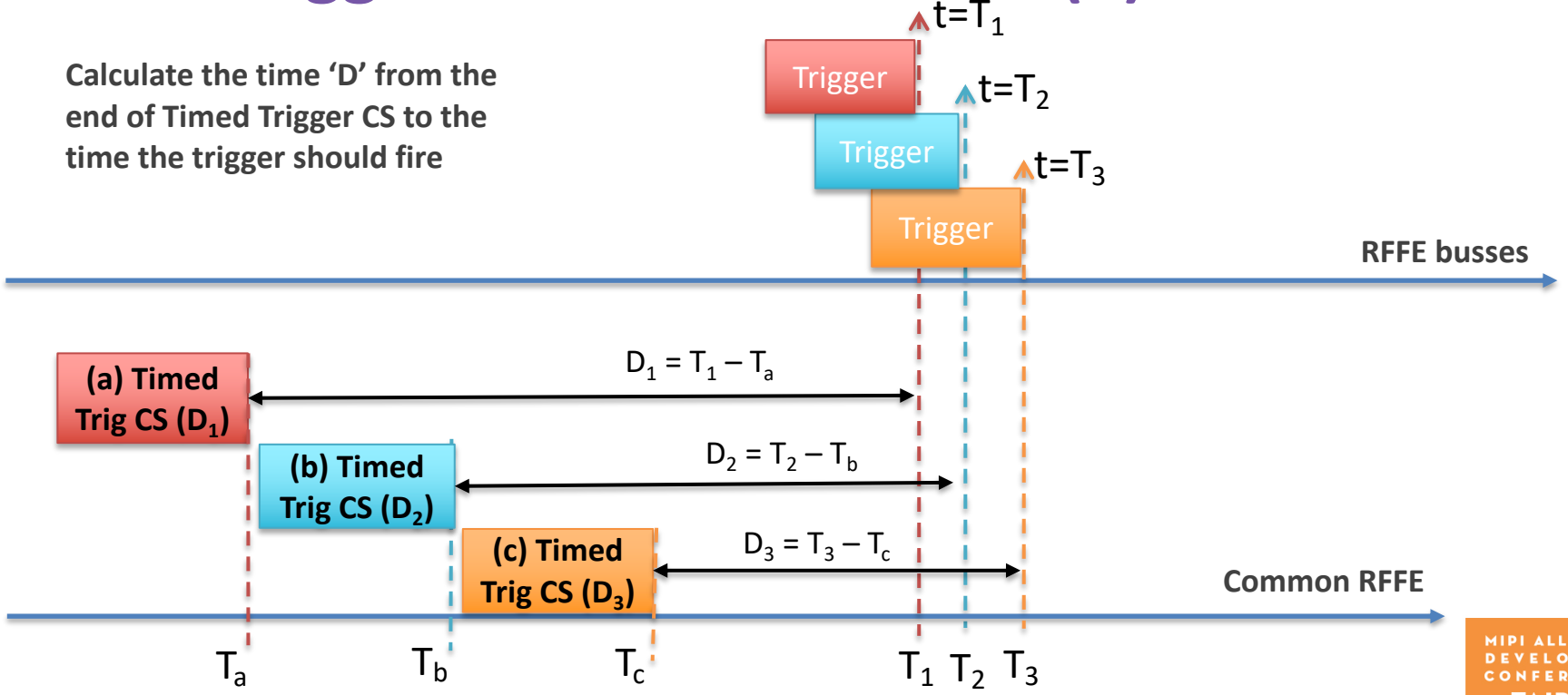
- How to solve the RFFE bus congestion with Timed Trigger(s)

Timed Trigger – Solution in Time (1)



Timed Trigger – Solution in Time (2)

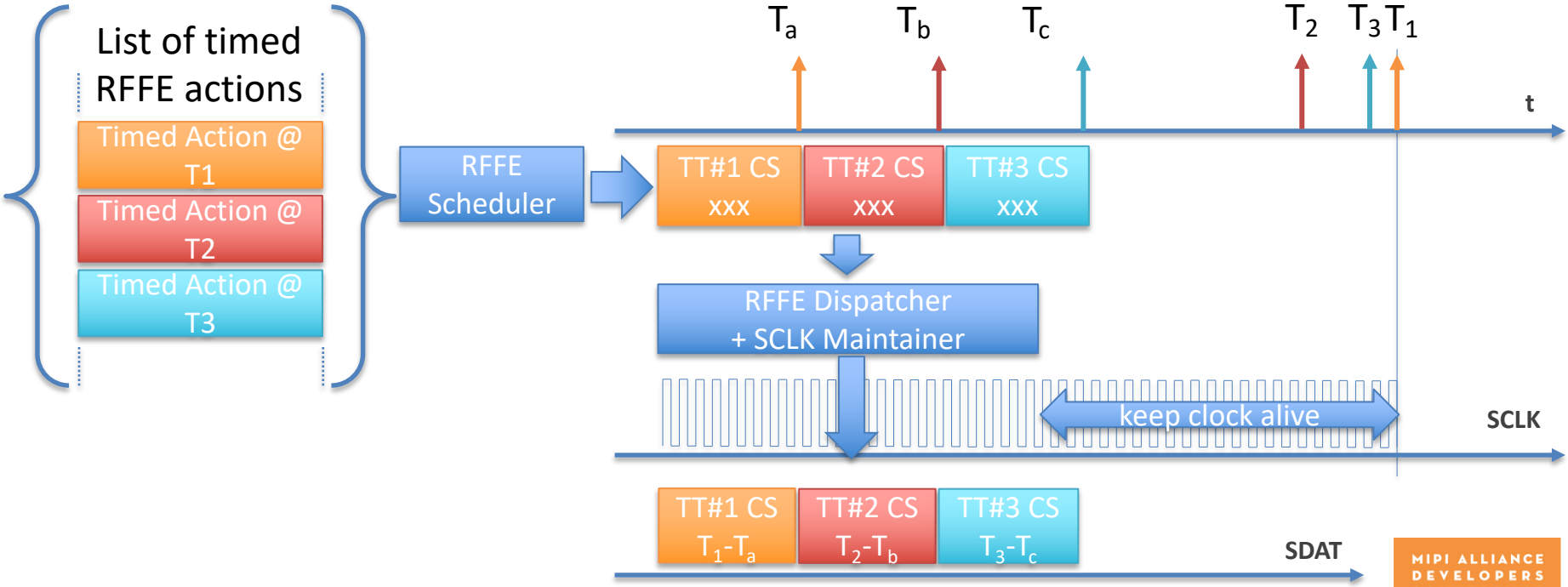
Calculate the time 'D' from the end of Timed Trigger CS to the time the trigger should fire



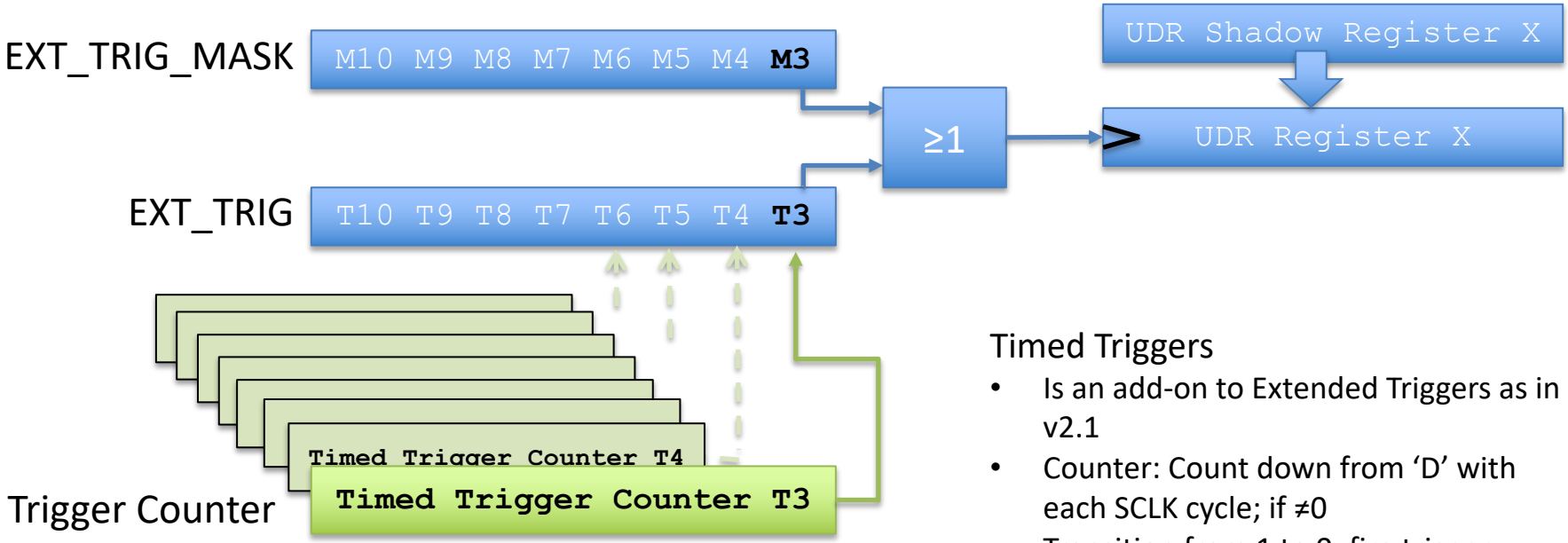
Design Topics

- How to design RFFE bus clients and masters

Adding Timed Triggers to RFFE Master Controller



Adding Timed Triggers to RFFE Client Controller



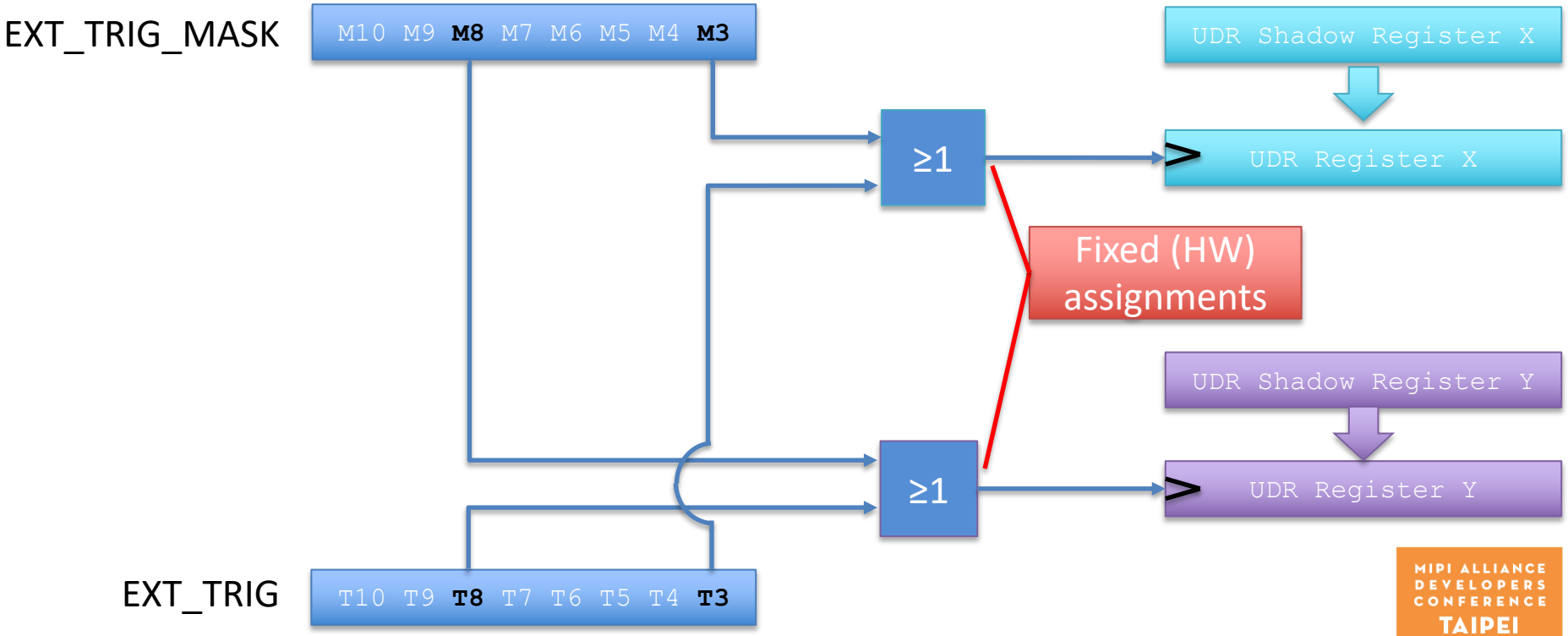
Timed Triggers

- Is an add-on to Extended Triggers as in v2.1
- Counter: Count down from 'D' with each SCLK cycle; if ≠0
- Transition from 1 to 0; fire trigger (Timer expired)

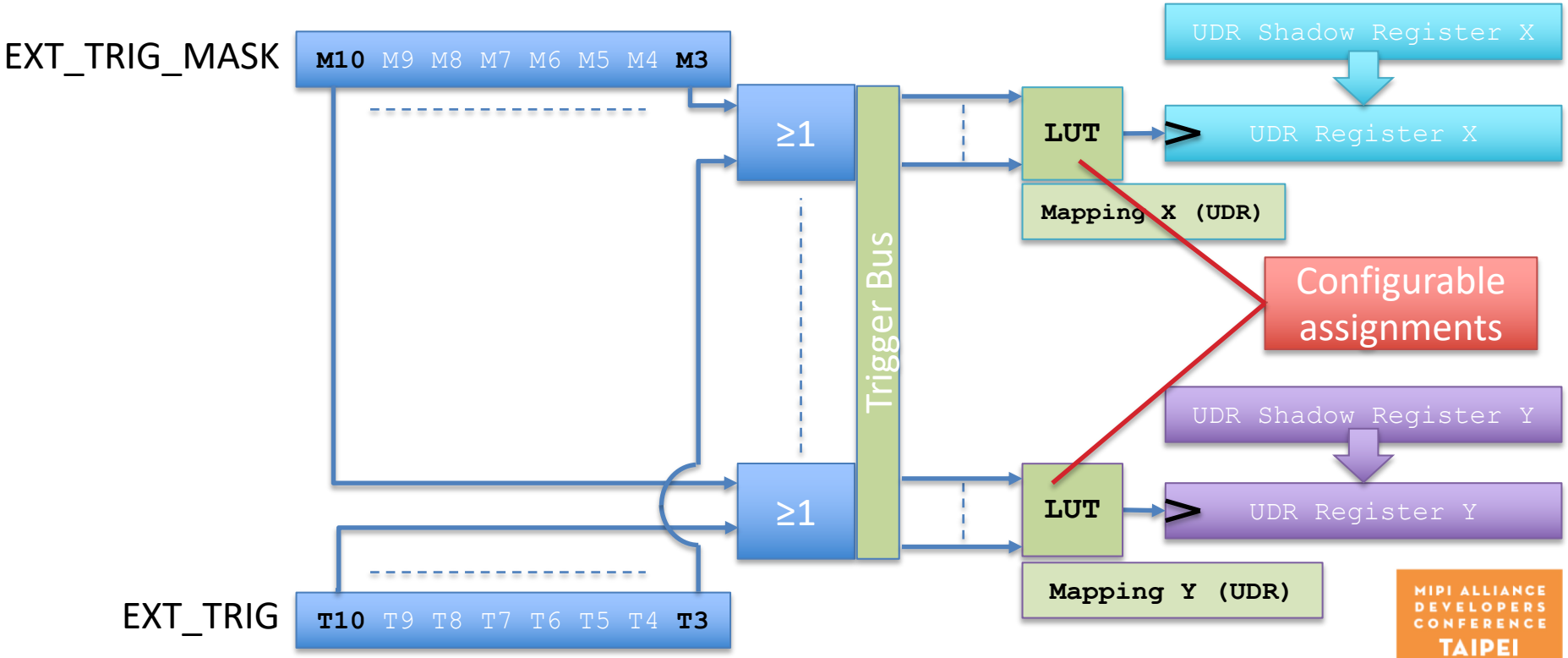
Mappable Triggers

- Problem to be solved
- Design issues

Problem: fixed assignment Trigger → UDR Register (Set)



UDR Register (Set) per LUT assigned to Trigger



Summary With Key Takeaway Messages

- Timed Triggers can reduced the number of RFFE busses
- Mappable Triggers can allow flexible mapping of Front End hardware to reduce the number of RFFE connection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