mipi® DEVCON

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A Developer's Guide to MIPI I3C℠ for Sensors and Beyond

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MIPI ALLIANCE
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CONFERENCE

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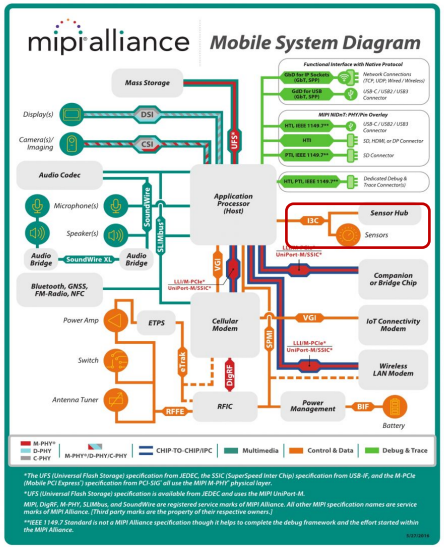
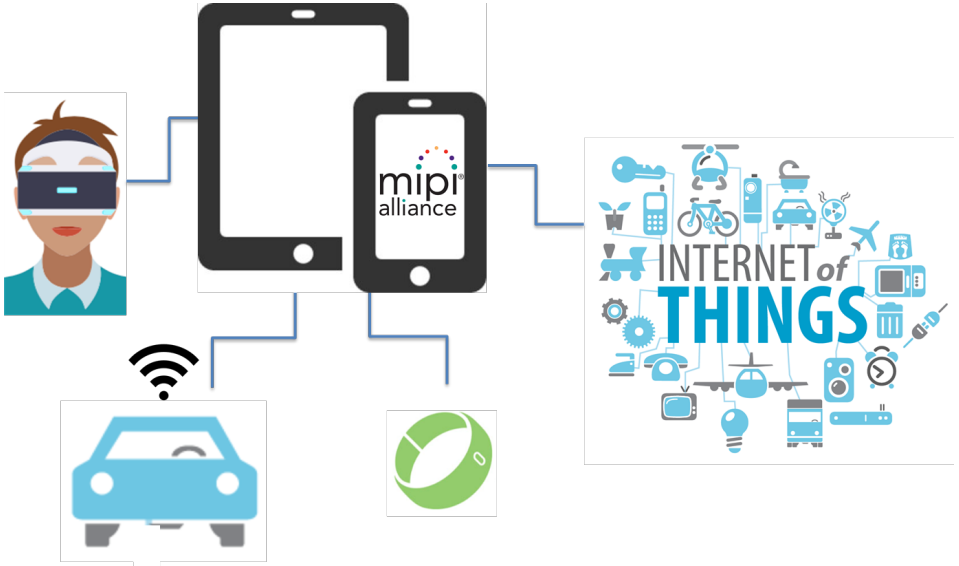
Outline

- Introduction to MIPI I3C℠
- Usages beyond sensing
  - MIPI Camera Control Interface (CCI℠)
  - MIPI Touch over I3C℠
  - MIPI Debug for I3C℠
- MIPI I3C℠ feature descriptions
- Implementation guidelines
  - Legacy Device Support
  - HDR Modes
  - Varied Topologies
- Summarized good design practices

MIPI I3C℠ for Ubiquitous Low Speed Interfacing

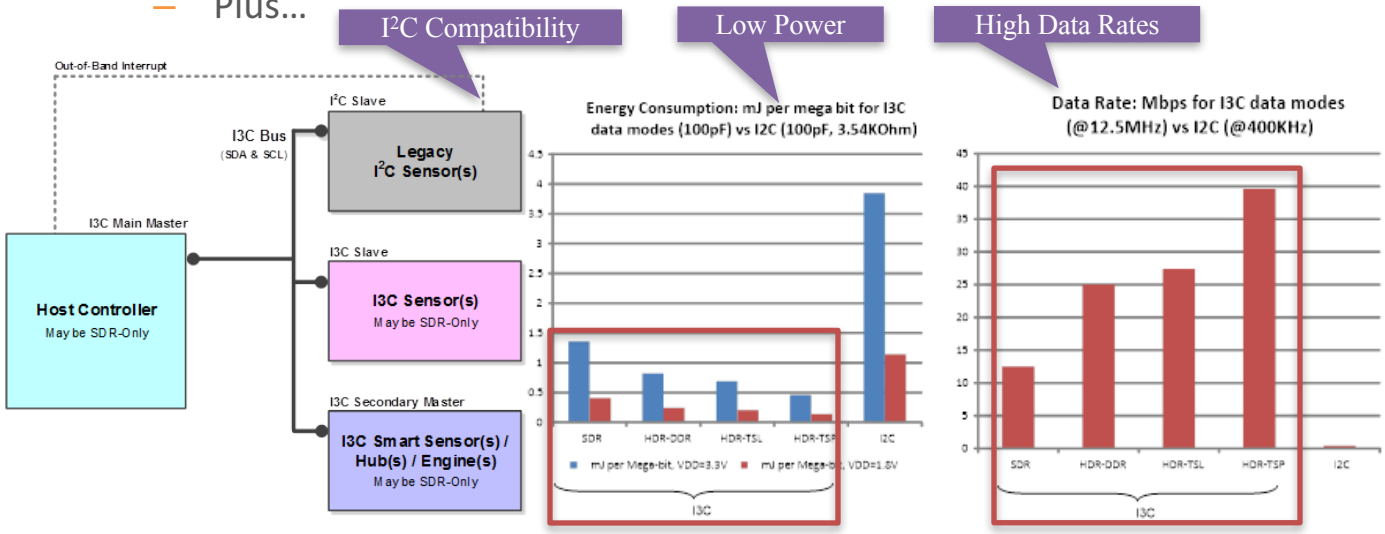
- Anywhere sensors are used, MIPI I3C℠ belongs
- Aimed toward historical I²C, SPI and UART applications in…



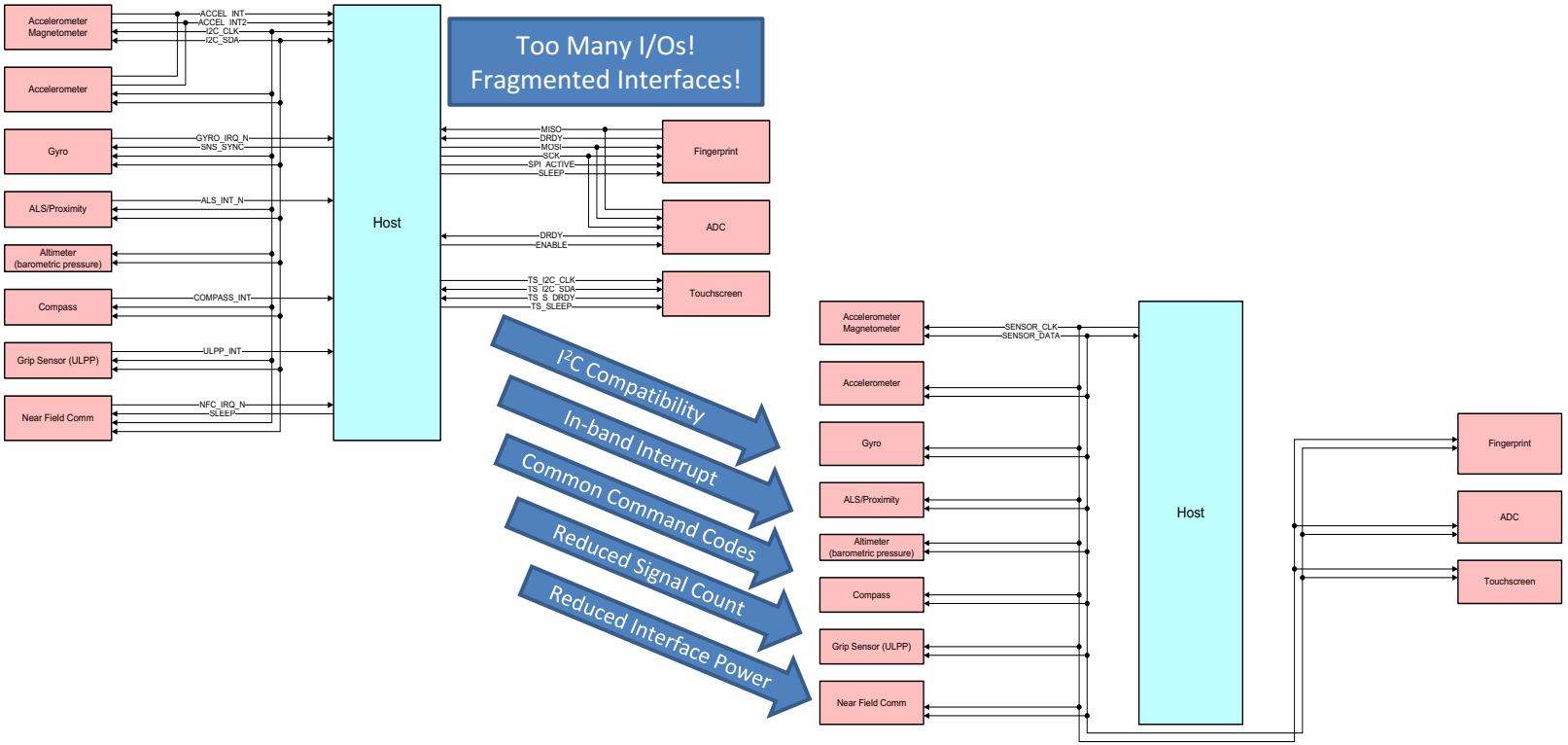


What is MIPI I3C℠?

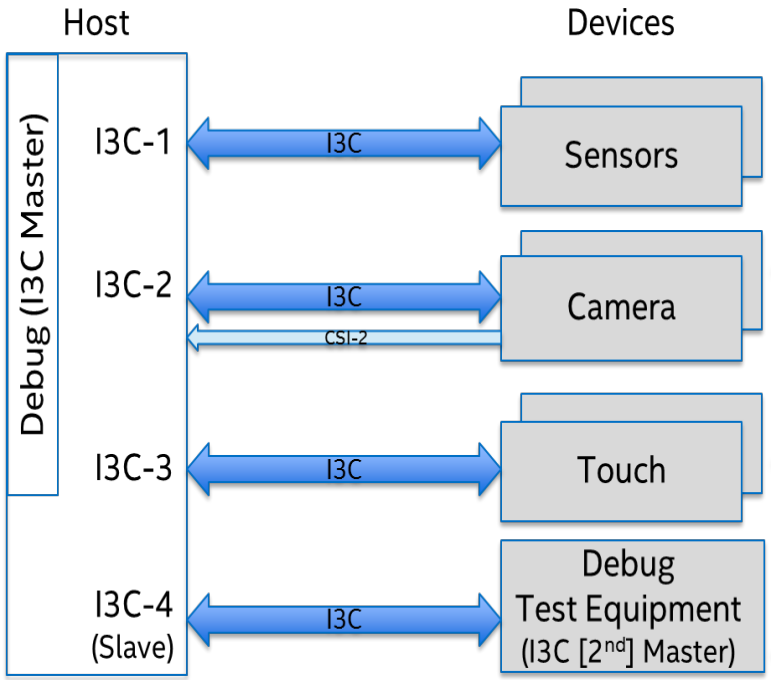
- Innovative new 2-Wire Sensor interface
- Key features address historical pain points
  - In-band Interrupt, Dynamic Addressing, Multi-Master, Standardized Commands, Time Control, Hot-Join, Error Detection and Recovery
  - Plus…



MIPI I3C℠ Vision?



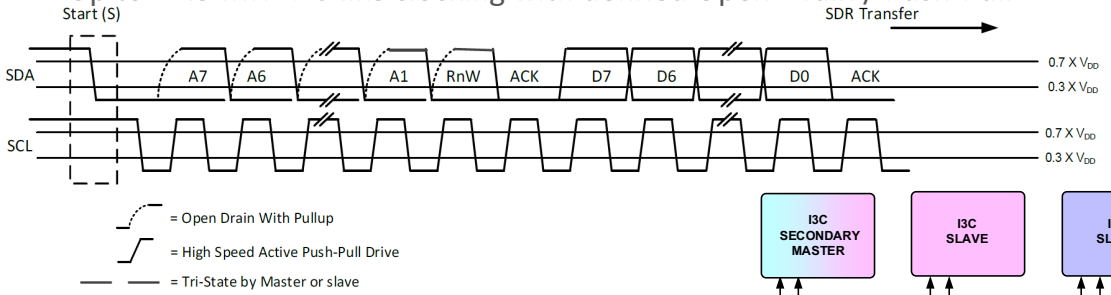
Usages Beyond Sensing



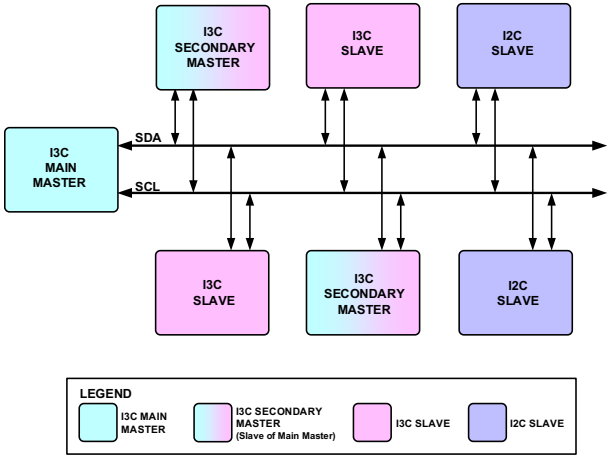
- MIPI CCI℠ (Camera Control Interface) over I3C℠ offers faster, lower latency and more efficient camera control with future abilities to support grouped data write and AON imaging
- Current touch screen controller interfaces are fragmented
- For many touch screens, MIPI Touch over I3C℠ presents a converged interface option for processed and raw touch data, leveraging IBI and HDR modes
- MIPI Debug for I3C℠ offers a more complete closed chassis, scalable and power aware platform debug capability with minimum boundary pin count

MIPI I3C^{SM} Features

- **I3C SDR – The Base Interface**
  - Up to 12.5 MHz I^{2}C-like clocking with defined Open-Drain / Push-Pull



  - Supports multiple classes of Devices
    - I3C Main Master
      - SDR-only Main Master
    - I3C Secondary Master
      - SDR-Only Secondary Master
    - I3C Slave
      - SDR-Only Slave
    - I^{2}C slave



MIPI I3C℠ Features

- **SDR Dynamic Address Assignment**
  - Standardized procedure for dynamic assignment of 7-bit Addresses to all I3C Devices
    - I3C Slaves have two standardized characteristics registers and an internal 48-bit Provisional ID to aide the procedure
  - Legacy I^2C Devices still use their static I^2C Address
- **SDR In-band Interrupt**
  - Slave device can issue START Request when in “Bus Available” state
  - Master provides Interface Clock for Slave to drive it’s Master-assigned address onto the bus
  - Lowest assigned address wins arbitration in Open-Drain configuration
  - A data payload (i.e. Mandatory Data Byte) can immediately accompany the In-band Interrupt

MIPI I3C℠ Features

- **Error Detection and Recovery Methodology**
  - For Master and Slave generated errors (9 Error Types identified, Parity, CRC5)
- **Common Command Codes**
  - Standardized command mode with extensible set of MIPI-defined codes that can be Broadcasted and/or Directed, Read and/or Write

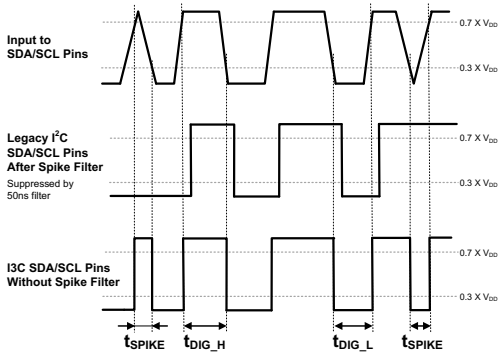
S or Sr	0x7E / W / ACK	Command Code / T	Data (Optional) (Broadcast CCC only) / T	Sr or P

* Example of Broadcast CCC Frame

  - Standardized Command Codes
    - Event Enable/Disable
    - Activity States
    - Payload Mgmt
    - I3C Feature Mgmt (Dynamic Address Assignment, Mastership, HDR Modes, Timing Control)
    - Test Modes
    - Extensible Space (MIPI and Vendor)

Guidelines - Legacy I²C Device Support

- Fm and Fm+ Speeds Supported
- 50ns Spike Filter (t_{SP}) Needed for 12.5MHz I3C^{SM} Clocking



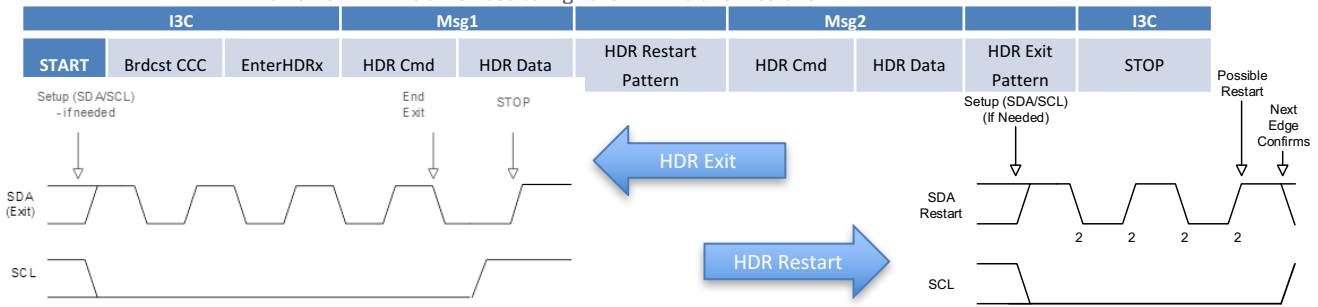
t_{SP}: pulse width of spikes that must be suppressed by the input filter

*UM10204: I2C-bus specification and user manual Rev. 6

- Clock Stretching is Not Allowed – I3C SCL is Push/Pull
- 20mA Open Drain Drivers (I_{OL}) are Not Used
- I²C Extended Addresses (10 bit) are Not Used

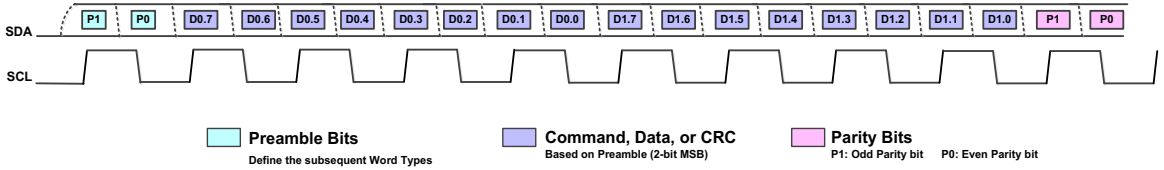
MIPI I3C^{SM} Features

- **I3C High Data Rate (HDR) Modes**
  - Optionally supported beyond the base SDR mode: 12.5MHz, SDA/SCL
    - HDR-DDR: Double Data Rate
    - HDR-TSL/TSP: Ternary Symbol
  - Offer bit rates over 33Mbps at a fraction of the per bit power of I^{2}C Fast Mode
  - Simple Slave-side digital implementations
  - Coexistent with legacy I^{2}C Devices
  - Leverage rising and falling edges
  - Individually entered using broadcasted MIPI-defined Common Command Codes
  - Universally exited and restarted via MIPI-defined toggling patterns
    - Allows non-HDR I3C Devices to “ignore” HDR transmissions

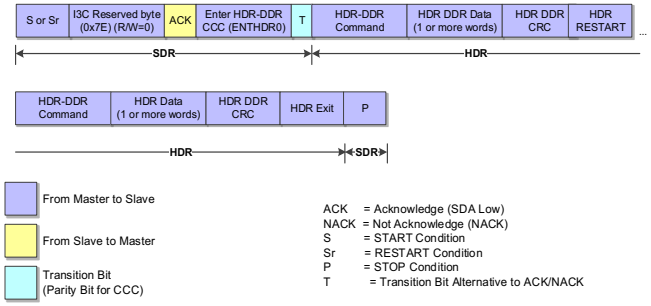


MIPI I3C℠ Features

- **HDR-DDR: Double Data Rate**
  - Uses SCL as a clock, however Data and Commands change SDA on both SCL edges. By contrast, SDR Mode changes SDA only when SCL is Low
  - HDR-DDR moves data by Words, which generally contains 2 preamble bits, 2 payload bytes and 2 parity bits. 4 Word Types defined: Command, Data, CRC, and Reserved

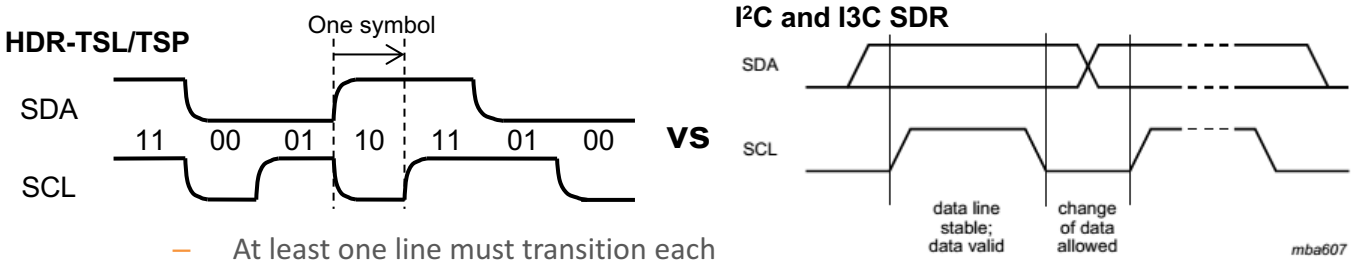


  - Simple protocol:



MIPI I3C^{SM} Features

- **HDR-TSL/TSP: Ternary Symbol Coding**
  - Ternary symbol coding for pure (TSP) and I²C legacy-inclusive (TSL) systems
  - Given a two-wire interface with 'simultaneous' transitions and no traditional clock, there are 3 possible symbols available – 0, 1, 2



  - At least one line must transition each
  - Ideally, there are 3 possible "next" transition
  - Transition indices are used to efficiently encode Binary into Ternary
  - Simple protocol:

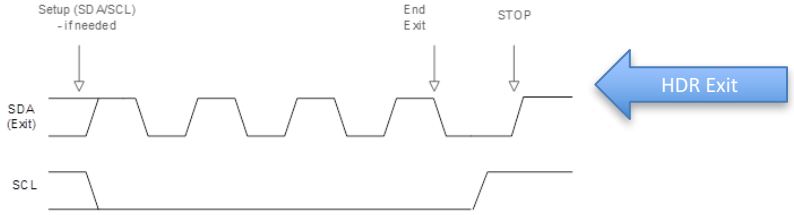
I3C SDR			Msg1			Msg2			I3C
START	Brdcst CCC	EnterHDRx	HDR Cmd	HDR Data	HDR Restart Pattern	HDR Cmd	HDR Data	HDR Exit Pattern	STOP

Guidelines - HDR Modes

- Enter HDR Commands Supported

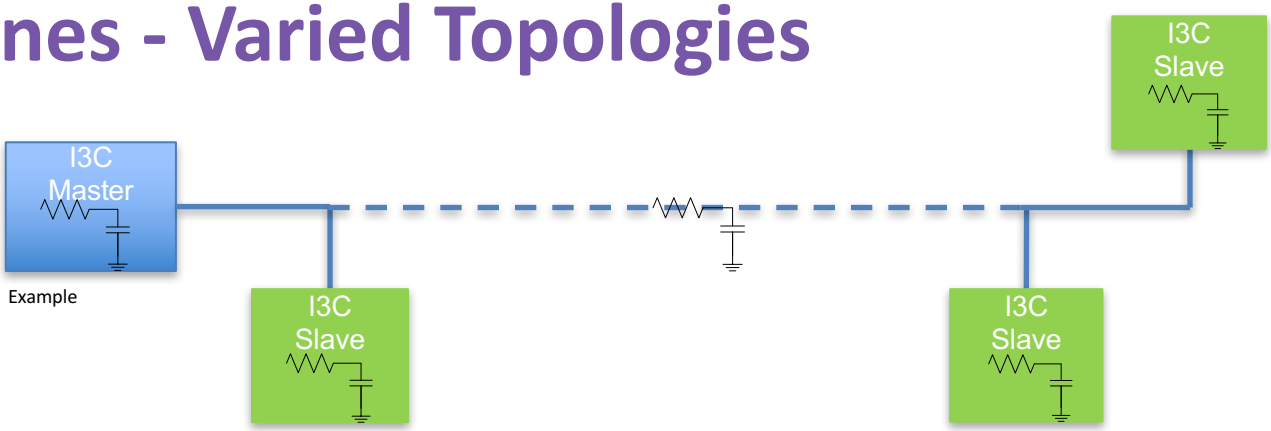
I3C			Msg1			Msg2			I3C
START	Brdcst CCC	EnterHDRx	HDR Cmd	HDR Data	HDR Restart Pattern	HDR Cmd	HDR Data	HDR Exit Pattern	STOP

- HDR Exit Pattern detected by all I3C Devices



- Non-HDR Devices shall ignore I3C HDR bus traffic until the HDR Exit Pattern is detected

Guidelines - Varied Topologies



- Impacts on signal transition/transit times (maximum bus frequency)
  - SDA/SCL drive strength: “weaker” for lower power and interference vs “stronger” for faster over larger topologies/loads
  - Trace length and material: short vs long and pcb vs cable
  - SCL/SDA pad capacitance
  - Clock to Data Turnaround Time (t_{SCO})
- Legacy I^2C Devices impact maximum bus frequency (MHz)
  - Must run I3C at speeds/pulses beyond Spike Filter or slow Bus to that of slowest I^2C Device
- Impacts on signal integrity/reliability
  - Device Location: close and far Devices can cause interference from reflections

Summarized Good Design Practices

- Thoroughly understand capability of coexistent Legacy I^2C Devices
  - 50ns Spike Filter
  - Disabled Clock Stretch
- Understand bus topology and performance tradeoffs Mixed (I3C and Legacy I^2C Devices) vs Pure Bus (I3C Devices Only)
  - Trace length and material
  - SDA/SCL pad capacitance
  - Clock to Data Turnaround Time (t_{SCO})
  - Device location

Any Questions?

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THANK YOU

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