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20-21 SEPTEMBER 2022

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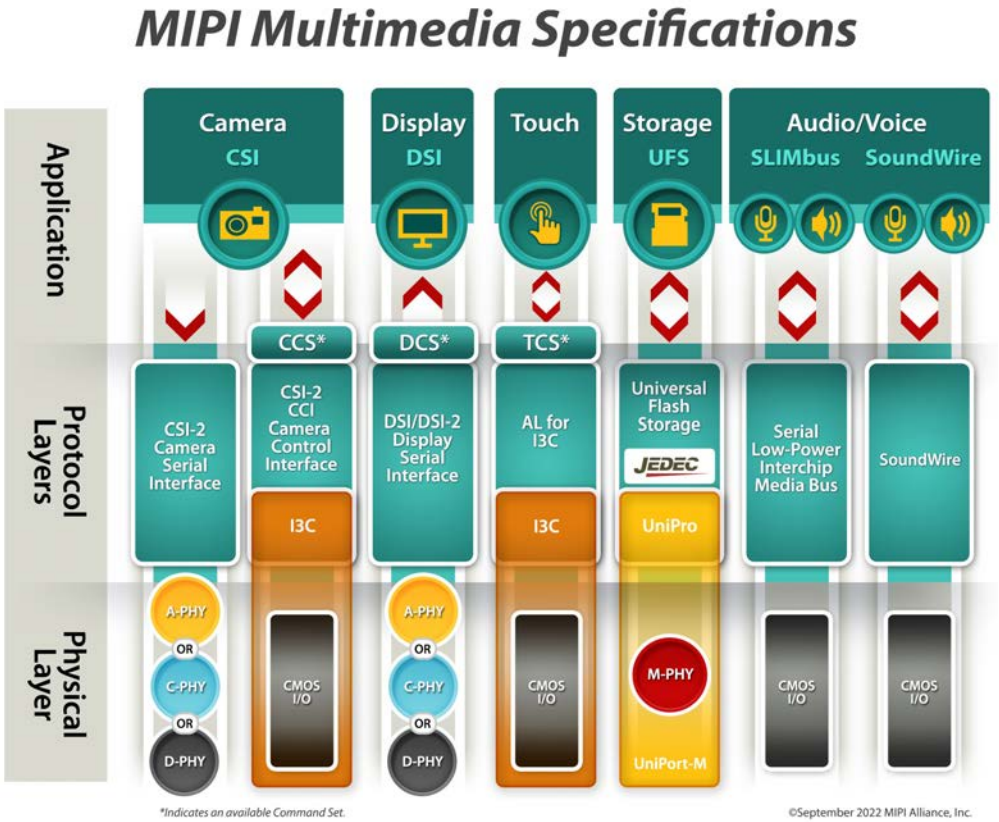
What's New and Coming Up on the MIPI PHY Roadmap

Agenda

- MIPI A-PHY® Future Plans
- MIPI D-PHY℠ Future Plans
- MIPI C-PHY℠ Future Plans
- MIPI M-PHY® Status/Future Plans

MIPI PHY's Ecosystems



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MIPI A-PHY® Future Plans

What is A-PHY?

The first industry-standard *long-reach* asymmetric SerDes physical layer specification targeted for ADAS/ADS surround sensor applications and infotainment display applications

A-PHY v1.0 offers:

- Direct coupling to native CSI-2/DSI-2/DP-eDP protocols
- High performance of up to 16 Gbps over 10-15m
- High noise immunity, ultra low PER (< 10^{-19})
- Supports bridge-based and endpoint integration
- Support for automotive coax and STP channels
- Power over cable
- Built-in Functional Safety according to ISO 26262

A-PHY v1.1 Enhancements:

- Increased support for lower cost legacy cables
- Double uplink data rate
- Star quad cable support, enabling dual downlink operation

PER: Packet Error Rate
STP: Shielded Twisted Pair
SPP: Shielded Parallel Pair
ADAS: Advanced Driver Assistance Syster
ADS: Autonomous Driving System
SoC: System On Chip

A-PHY Feature Roadmap

Category	Feature	v1.0	v1.1[2]	V2.0	Next
	Board Adoption	Q3 20	Q4 21	Q2 23	24-25
Channels	Coax Channel 15 meter – 4-inline connectors	✓	✓	TBD	TBD
	STP / SPP Channel 10 meter – 4 inline connectors	✓	✓	TBD	TBD
	STQ 10 meter – 4 inline connectors (2 differential pairs)	-	✓	TBD	TBD
Max Downlink Data Rate	Single Lane Downlink	16Gbps	16Gbps	32Gbps	>48Gbps
	Dual Lane Downlink	-	32Gbps	64Gbps	~100Gbps
Max Uplink Data Rate	Uplink	100Mbps	200Mbps	1.6Gbps	TBD
Power Over Cable	Power over Coax and Power over Data Line – Max power delivery	6W	6W	10W[1]	TBD[1]
EMC Requirements	RF Ingress (ISO 11452-2)	✓	✓	✓	✓
	Bulk Current Injection (ISO 11452-4)	✓	✓	✓	✓
	Fast Transient (ISO 7637-2/3)	✓	✓	✓	✓
	Alien Cable bundle cross talk	✓	✓	✓	✓
	Car Noise	✓	✓	✓	✓
Advanced features	Modulations: NRZ, PAM4, PAM8, PAM16	✓	✓	✓	✓
	Just-In-Time-Canceller & Retransmission	✓	✓	✓	✓
	Packet Error Rate	10^{-19}	10^{-19}	10^{-19}	10^{-19}
	Max Link Latency @ G5 (16Gbps)	~6uSec	~6uSec	TBD	TBD
	Functional Safety (ISO 26262) – Message Counter, CRC, Timeout monitoring	✓	✓	✓	✓
Data Link Layer	Local Functions, Multi-Port Functions, Network Functions	✓	✓	✓	✓
	BIST	✓	✓	✓	✓
	Clock Forwarding Service	✓	✓	✓	✓
	Timebase Service	-	✓	✓	✓

Note:

(1) Power over cable will be defined in the PoA specification (separated from A-PHY specification)

(2) A-PHY v1.1.1 will replace v1.1 with inclusive terminology update

A-PHY Feature Roadmap

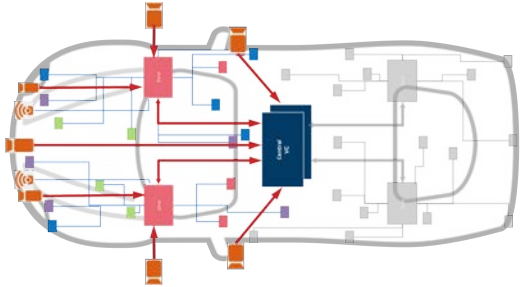
Category	Feature	v1.0	v1.1	V2.0	Next
Control and Management	ACMD – A-PHY Control and Management Database	✓	✓	✓	✓
	ACMP – A-PHY Control and Management Protocol	✓	✓	✓	✓
	ACMPn – additional ACMP modes (e.g. CCISE)	-	✓	✓	✓

A-PHY PAL Roadmap

Category	Feature	A-PHY v1.0	A-PHY v1.1	A-PHY Next
A-PHY	Board Adoption	Q3 20	Q4 21	~2022/23
Protocols Adaption Layers	PAL/CSI-2	v1.0	v1.1 (Q1/22)	
	PAL/DSI-2	v1.0		
	PAL/eDP-DP	v1.0		
	PAL/GPIO	v1.0		
	PAL/I2C	v1.0(1)		
	PAL/Ethernet		v1.0 (Q1/22)	
	PAL/I3C		TBD	
	PAL/SPI		v1.0 (Q3/22)	

Note:
(1) PAL/I2C v1.0.1 will replace v1.0 with inclusive terminology update

A-PHY-Based Zonal Architecture



- Simplification of zonal ECU
  - Low computing overhead
  - Lower protocol overhead – Maintain native protocols for MIPI CSI-2 (e.g., camera) or Ethernet (e.g., lidar)
  - Designed for ultra-low PER at high noise environment for the entire lifespan of the vehicle
- Future-looking design and easy migration path
  - Scalable downlink speed from 2Gbps to 64Gbps over a single cable
  - Flexible and rich protocol support
  - Layered security scheme supporting variety of use cases
  - Embedded functional safety
- Guaranteed interoperability and backward/forward compatibility

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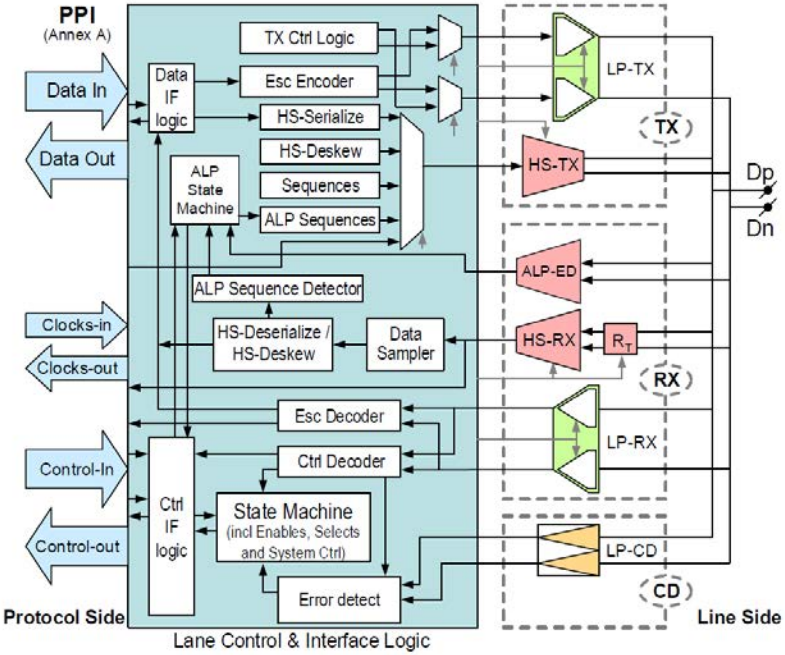
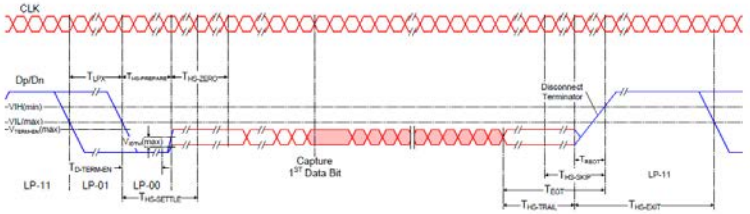
MIPI D-PHY℠ Future Plans

What is D-PHY?





- D-PHY is a Physical Layer targeted for Camera and Display applications.
- D-PHY is already in many mobile devices interfacing Camera and Display modules.
- D-PHY is targeted for short to medium reach applications.

D-PHY Feature Roadmap

Category	Feature	v1.0	v1.1	v1.2	v2.0	v2.1	v2.5	v3.0
	Board Adoption	4Q 09	4Q 11	3Q 14	1Q 16	1Q 17	3Q 19	3Q 21
Symbol Rate (Gbps/Lane)	Standard Channel	1	1.5	2.5	4.5	4.5	4.5	9
	Short Channel					6.5	6.5	11
Increased Symbol Rate	Basic De-emphasis				✓	✓	✓	✓
	Calibration			✓	✓	✓	✓	✓
	Additional UI Jitter (RCLK jitter) specs		✓	✓	✓	✓	✓	✓
	Rx Equalization							✓
Power Reduction	Unterminated Mode				✓	✓	✓	✓
	Reduced Amplitude “LVLP” Mode option					✓	✓	✓
LP Mode	Alternate Low-Power Mode						✓	✓
Enhanced Function	16-bit/32-bit PPI				✓	✓	✓	✓
	Optical Interconnect				✓	✓	✓	✓
	HS Reverse Mode	✓	✓	✓	✓	✓	✓	✓
	PHY Generated/Detected Packet Delimiter					✓	✓	✓
	Fast Lane Turnaround						✓	✓
	4m channel support, for IoT use cases				✓	✓	✓	✓
Protocol Specs	MIPI CSI-2®			v1.2/ v1.3		v2.0	v3.0	v4.0
	MIPI DSI-2℠	-	-	v1.1/ v1.0	v2.0	-	-	-

D-PHY Feature Roadmap

Category	Feature	v3.0	v3.5 FC	v3.5 EC (Optional)	v4.0 EC (Tentative)
	Board Adoption	3Q 21			
Symbol Rate (Gbps/Lane)	Standard Channel	9	9	9 Bands B1, B2, B3, B4	TBD
	Short Channel	11	11	Same as above	TBD
Increased Symbol Rate	Basic De-emphasis	✓	✓	✓	✓
	Calibration	✓	✓	✓	✓
	Additional UI Jitter (RCLK jitter) specs	✓	✓	✓	✓
	Rx Equalization	✓	✓	✓	✓
Power Reduction	Unterminated Mode	✓	✓	X	TBD
	Reduced Amplitude “LVLP” Mode option	✓	✓	✓	✓
LP Mode	Alternate Low-Power Mode	✓	✓	X	TBD
Enhanced Function	16-bit/32-bit PPI	✓	✓	✓	✓
	Optical Interconnect	✓	✓	✓	✓
	HS Reverse Mode	✓	✓	X	TBD
	PHY Generated/Detected Packet Delimiter	✓	✓	✓	✓
	Fast Bus Turnaround	✓	✓	X	TBD
	4m channel support, for IoT use cases	✓	✓	✓	✓
Protocol Specs	CSI-2	v4.0			
	DSI-2	v2.0	v2.1	v2.1	v3.0

Specification under development phase

- D-PHY 3.5 include
  - Supports an optional Embedded Clock configuration.
  - Embedded clock configuration has better EMC compliance and provides additional lane for data communication. Improves total data throughput.
  - Embedded Clock mode supports up to 9 Gbps.
  - Forwarded Clock configuration is carried forward from D-PHY 3.0.
  - Forwarded Clock mode, fully backward compatible to D-PHY 3.0.
  - ALP mode not supported in Embedded Clock mode.
  - Support of 4 meter of channel for IOT applications.
  - Targeted for Camera and Display protocols.

Overall possibilities

- Future plans of D-PHY 4.0 include
  - Taking data rates to around 18 to 20 Gbps.
  - Still keeping it NRZ.
  - LP model to be removed. ALP mode to be primary mode.
  - Support mid length around 4 meter of channel for IOT applications.
  - Will not be fully backward compatible to D-PHY 3.5.
  - Will be targeted for Camera and Display protocols.

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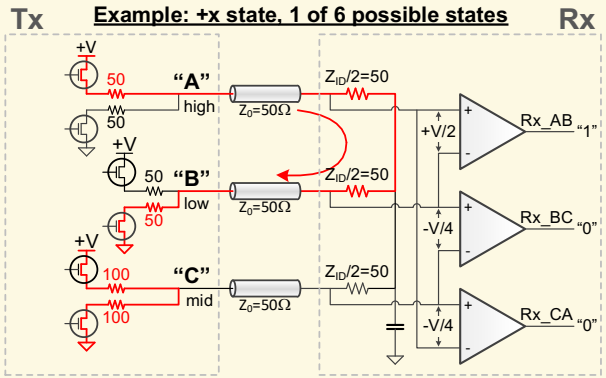
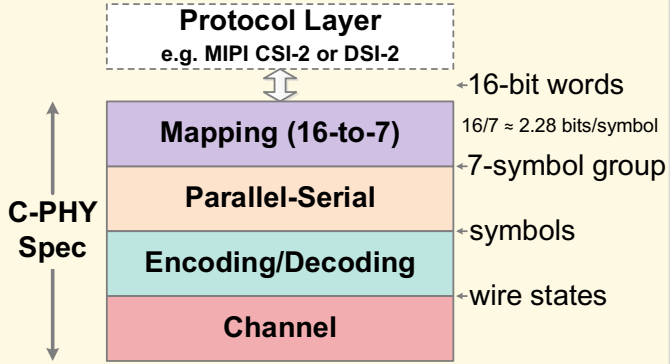
MIPI C-PHY℠ Future Plans

What is C-PHY?

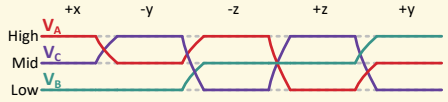




Benefits of 3-Phase Coding

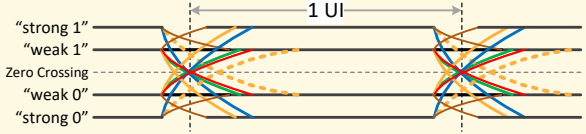
- High bit rate: 2.28x sym. rate
- Low power consumption
- Low signal toggle rate
- No clock signal emissions
- Fewer Lanes required, fewer connections in a system
- Flexibility to assign Lanes to a specific camera or display Link

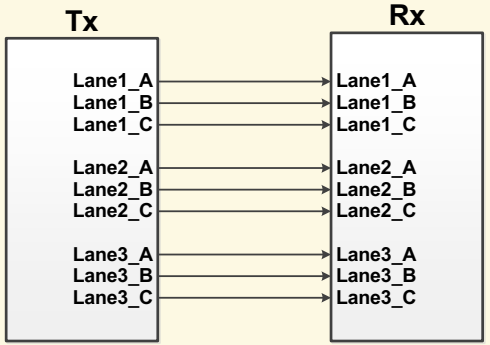
Single-Ended at Tx



6 states, a transition at every UI to 1 of 5 others, $\log_2(5) \approx 2.32$ bits/symbol

Differential at Rx



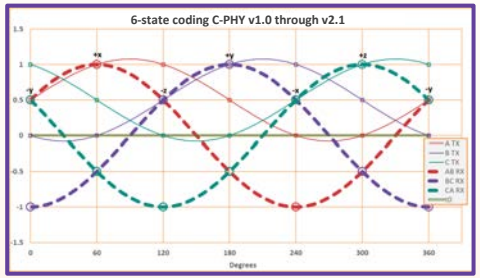


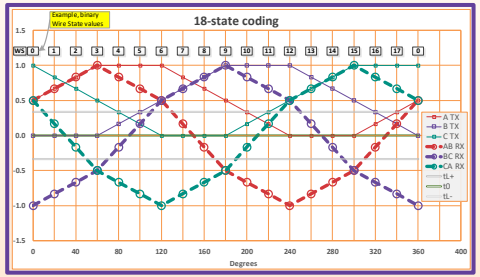
C-PHY Feature Roadmap

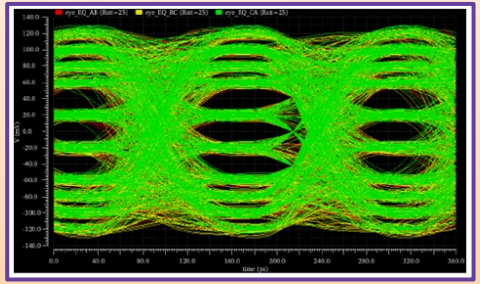
Category	Feature	v1.0	v1.1	v1.2	v2.0	v2.1	v3.0
	Board Adoption	4Q 14	1Q 16	1Q 17	3Q 19	3Q 21	~1Q 23
Symbol Rate (Gsps/Lane)	Standard Channel, Gsps (Gbps)	-	2.8 (6.4)	3.5 (8.0)	6 (13.7)	6 (13.7)	~5 (17.8)
	Short Channel, Gsps (Gbps)	-	3.0 (6.9)	4.5 (10.3)	8 (18.3)	8 (18.3)	~7 (24.9)
Increased Symbol Rate	Basic Pre-emphasis		✓	✓	✓	✓	✓
	Advanced TxEQ, Calibration Additional UI (RCLK) Jitter specs			✓	✓	✓	✓
	Rx Equalization				✓	✓	✓
	Multi-phase 18-state coding (3.556 coding factor)						✓
Power Reduction	Unterminated Mode		✓	✓	✓	✓	✓
	Reduced Amplitude “LVHS” Mode option			✓	✓	✓	✓
LP Mode	Alternate Low-Power Mode			✓	✓	✓	✓
Enhanced Function	16-bit/32-bit PPI		✓	✓	✓	✓	✓
	16-bit/32-bit/64-bit PPI					✓	✓
	HS Reverse Mode			✓	✓	✓	✓
	Sync Word Selection to enhance Scrambling			✓	✓	✓	✓
	PHY Generated/Detected Packet Delimiter			✓	✓	✓	✓
	Fast Lane Turnaround				✓	✓	✓
	4m channel support, for IoT use cases				✓	✓	✓
	MIPI terminology update					✓	✓
	Guidance for LVHS mode with CTLE.						✓
	Investigate: multipoint, ALP noise margin, testing update						✓
Protocol Specs	MIPI CSI-2®	v1.3	-	v2.0,2.1	v3.0	v4.0	TBD
	MIPI DSI-2℠	-	v1.0	v1.1	-	v2.0	TBD

C-PHY v3.0 Preview

- Timeline: anticipated WG completion ~1Q 2023
  - v3.0 spec development is the primary task in the C-PHY WG
- Increased coding factor enabled by 18-state coding
  - Higher coding efficiency, more bits-per-symbol, coding for reduced RX jitter
  - Simulations show lower emissions with 18-state coding
  - New coding, mapping, calibration, new special code words, eye diagram
- Compatibility with prior C-PHY versions
  - 6-state mode and LP signaling are still supported, 18-state mode is optional
- Improved margins for ALP mode
- Multipoint support for camera
- Guidance for LVHS reduced-level mode with CTLE
- Enhancements to existing Built-in Test capability
- Interconnect design guidelines app note, a companion document to v3.0







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MIPI M-PHY® Status/Future plans

M-PHY introduction

- What is M-PHY?
  - Is a versatile physical layer targeting applications with a particular need for high data rates, low pin counts, lane scalability and power efficiency
  - M-PHY is the base physical layer of JEDEC UFS 2.0, 3.0 and new 4.0.
  - Poised to be dominant Mobile Storage interface deployed in 5G-enabled Smartphones
- Why M-PHY was created
  - To meet the constant demand for efficient high-speed communications in mobile ecosystem
- What M-PHY is used for
  - Flash memory storage and chip to chip communication applications for mobile/mobile influenced and automotive ecosystems

M-PHY Key features

- Fifth generation mobile physical layer
- High performance with peak transmission rate of 23.32Gbps per lane (M-PHY v5.0)
- Low power, low latency efficient architecture, excellent for battery powered, mobile and mobile influenced systems.
- Low EMI
- Optimized for advanced storage
- Extensive debug features

M-PHY Feature Roadmap

Category	Feature	v2.0	v3.1	v4.1	v5.0	v6.0
	Board Adoption	Q2 12	Q2 14	Q1 17	~Q4 21	~2025
Data rate	Max data rate per lane (Rate B Gbps)	~3	~6	~12	~24	TBD
Channel support	Mobile Long Channel (CH2, channel length in inches)	~13	~13	~13	-	-
	Mobile Standard Channel (CH1, channel length in inches)	~6	~6	~6	~6	~6
	Automotive Channel					TBD
Equalization	Tx De-emphasis		✓	✓	✓	✓
	Rx Equalization			✓	✓	✓
	Advanced Tx and RX equalization					✓
Power Reduction	Unterminated Mode	✓	✓	✓	-	-
	Burst mode transmission	✓	✓	✓	✓	✓
LP Mode	H8 using SQ operation	✓	✓	✓	✓	✓
Enhanced Function	High speed start up				✓	✓
	Low speed start up	✓	✓	✓	✓	-
	Low speed signaling	✓	✓	✓	✓	-
	Eye monitor				✓	✓
	Shared reference clock only				✓	✓
	PAM4 or shorter channel NRZ (need feasibility)					TBD
	Timing parameters updates		✓	✓	✓	✓
	Advanced training					TBD
	FEC or other error correction (if PAM4 will be chosen)					TBD
	Data-rate adjustments for integer PLL				✓	✓
	Frequency Offset PPM differences minimized				✓	✓
Protocol Specs	MIPI UniPro®	v1.4	**v1.6**	v1.8	v2.0	v3.0
	UFS	v1.0	v2.0	v3.0/3.1	v4.0	v5.0

M-PHY Future plans

- What is next for M-PHY
  - M-PHY six's generation development is about to start
  - Targeting bandwidth increase and throughput enhancement
  - Penetrating new ecosystems and utilizing new use cases
  - Backward compatibility is a key pathway

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THANK YOU!

ADDITIONAL RESOURCES

- MIPI A-PHY, learn more:
  - https://www.mipi.org/specifications/a-phy
- MIPI C-PHY, learn more:
  - https://www.mipi.org/specifications/c-phy
- MIPI D-PHY, learn more:
  - https://www.mipi.org/specifications/d-phy
- MIPI M-PHY, learn more:
  - https://www.mipi.org/specifications/m-phy

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Q&A