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IF IT'S NOT MIPI, IT'S NOT MOBILE

Achieving Optimal Energy and Power Efficiency with MIPI I3C®

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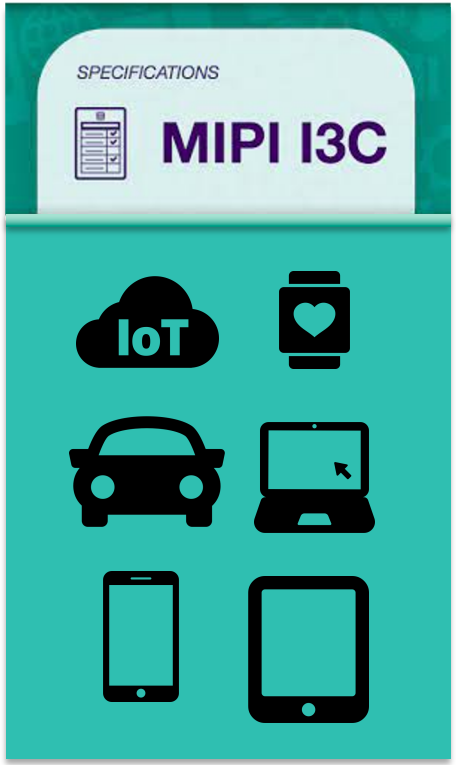
Agenda

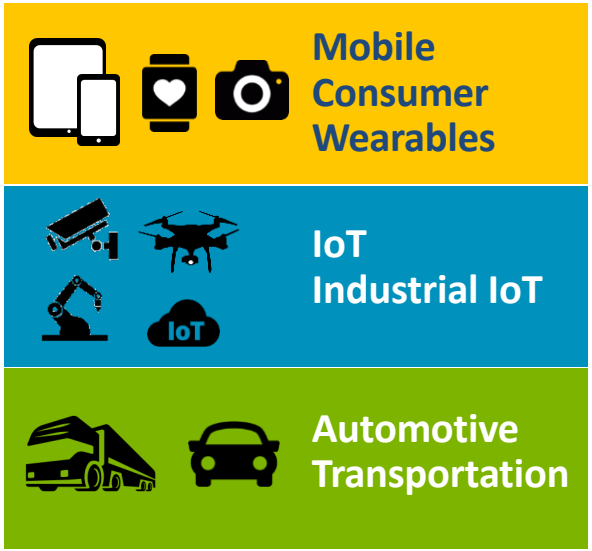
- I3C / I3C Basic Introduction
- Power and Energy Performance Improvements
- I3C Bus Transactions
- Additional Resources
- Q & A



I3C / I3C Basic Introduction

MIPI I3C Interface - Introduction

Fast Growing Sensor Markets



Smarter, more capable

Avg >20 sensors/device (projected)

- Accelerometer
- Gyroscope
- Magnetometer
- Ambient light
- Pressure
- Humidity
- Temperature
- .. others

I3C a scalable, cost-effective interface

- Targeting mobile & IoT devices, automotive, server manageability
- Simplify connecting and managing multiple sensors in a device
- Reduced pin count and signal paths
- CMOS I/O Compatible
- Support for low-power, high-speed communication (vs. I2C/SPI/UART)
- Low complexity target
- Compatibility with I2C devices

The MIPI I3C Interface Ecosystem

SPECIFICATIONS

I3C v1.1.1

- Available to MIPI members
- FAQ & several Application Notes available
- Released Jun 2021

I3C Basic v1.1.1

- Rich subset of I3C
- Feature list here
- Publicly available by complying to MIPI IPR
- Released Jul 2021

SOFTWARE & TEST

I3C HCI v1.1

Host Controller Interface

- Facilitates connection of peripheral devices to an application processor
- Publicly available to developers and the open-source community
- Available in mainstream Linux kernel tree (v5.x)

I3C CTS v1.0

Conformance Test Suite

- Improves interoperability among different products
- Strong focus on SDR-only bus transactions, error detection and recovery
- Continuous evolution by expanding test scopes

INTEGRATION

- Debug for IoT v1.0
- DisCo for I3C
- I3C over Camera interface
- JEDEC – SPD (Serial Presence Detect)
- DMTF - MCTP I3C Transport Binding Specification
- ETSI for Smart Secure Platform
- PCIe sideband (WIP)
- More to come!

MIPI I3C Key Features

Fast Efficient Communication Channel

- Multidrop SDA/SCL 2-wire interface
  - 12.5 MHz max clock rate
  - 1.2V-3.3V Voltage supported
- Dynamic switch between pull-up/push-pull/Hi-Z
- Line coding modes for higher throughput:
  - SDR, HDR-, HDR-TSL, BT
  - Multilane x2, x4
- Low EMI
- Physical layer CMOS I/O compatible

System Management

- Primary & Secondary Controllers
- Dynamic Address Assignment including Group Addressing
- Device Code Assignment (by MIPI)
- Descriptors:
  - **DCR** Device Configuration Register
  - **BCR** Bus Configuration Register
  - **SETBUSCON** Bus Context Operation

Advanced Functions

- Multi-operation via repeated START
- Unicast, Broadcast, Multicast messages
- In-Band Interrupt with qualified information
- Device reset
- Hot-join
- Error detection (parity, CRC)

Backward Compatibility

- Mixed-bus operation: I3C and I2C devices
  - Static address space reserved for I2C legacy devices
- Fast operations invisible to I2C thanks to 50 nanosecond spike filter

Introduced in v1.1

Power and Energy Performance Improvements with I3C

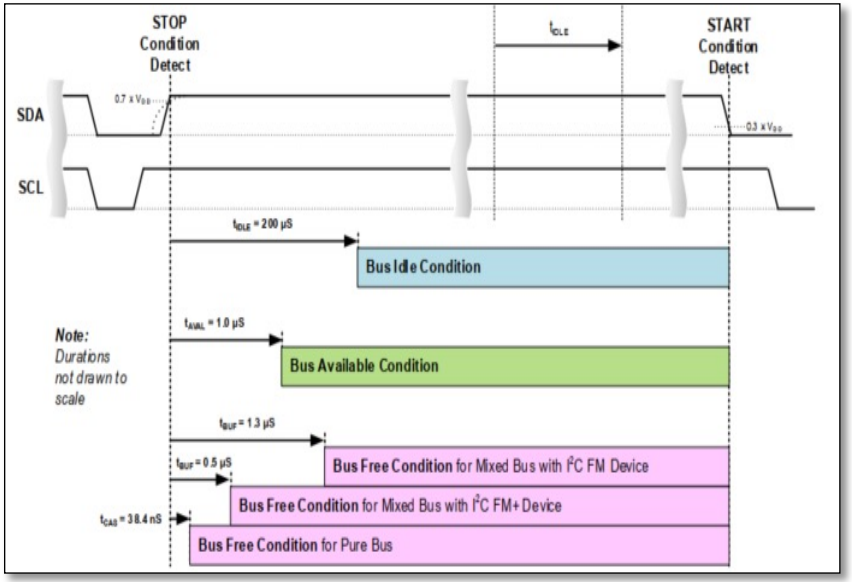
Need for Power/Energy Efficiency in IoT Devices

- **Many classes of IoT devices work under tight power budget (wearables, in-file data collection units, etc.)**
- **Low energy consumption and power efficiency are key features**
  - Low-voltage operation
  - Running on battery
  - Non-rechargeable, targeting several years operation
- **I3C can help solve above challenges**
  - Excellent bus electrical characteristics
  - Handling of synchronous and asynchronous events
  - Selective power management of sub-components
  - System segmentation

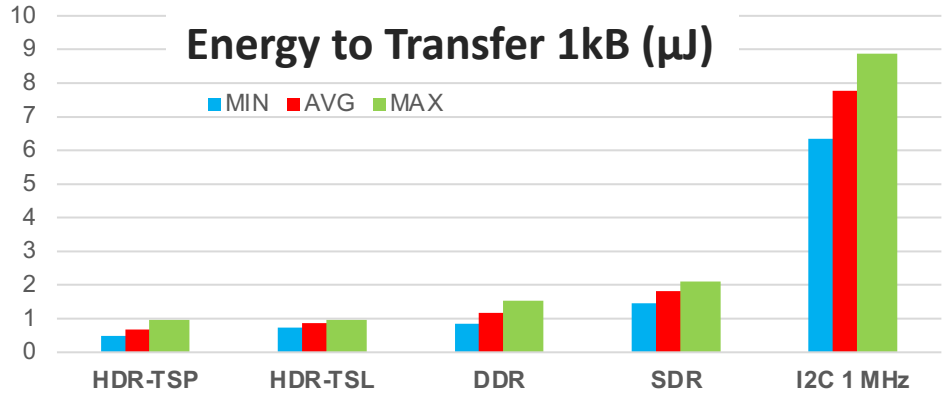
I3C features & specs are great help to system designers to architect Power Efficient IoT Devices for their next projects

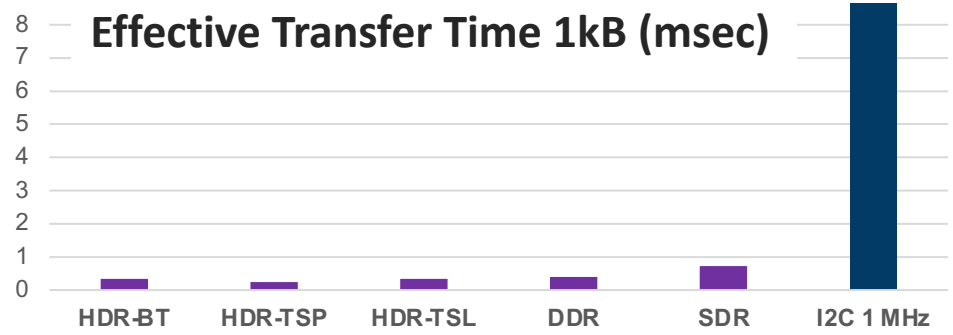
I3C Bus - Low Energy & Power Features

- **Simple 2-wire interface**
  - helps to keep component count
  - Reduced wire spurious capacitance
- **Operating voltage: 1.2V - 3.3V**
  - Low operating voltage allows use of lowest-voltage components
- **Efficient bus transactions operation**
  - Minimize energy used per bit sent
  - Reduced number of signal transaction
  - Use of Push-Pull driver whenever possible
- **Enable system-level power-efficient architecture**
  - In-Band Interrupt for efficient data acquisition
  - Management of Bus Idle States



Bus Performance for 1kB Transfers





Energy & Transfer Time Improvement vs. I2C

- Energy Reduction
  - SDR Mode: 4.3 times lower
  - HDR-TSP mode: 18 times lower
- Faster Transfer Time
  - SDR mode: 11 times faster
  - HDR-TSP: 33 times faster

Improving Idle-time with Bus Conditions

Informing Targets of bus idle condition facilitates low power management

- Specific CCC allocated: ENTAS[0..3]
- ENTASx informs Target(s) about low activity intervals
  - 2ms & 50ms idle time can rack up significant power savings

Remark

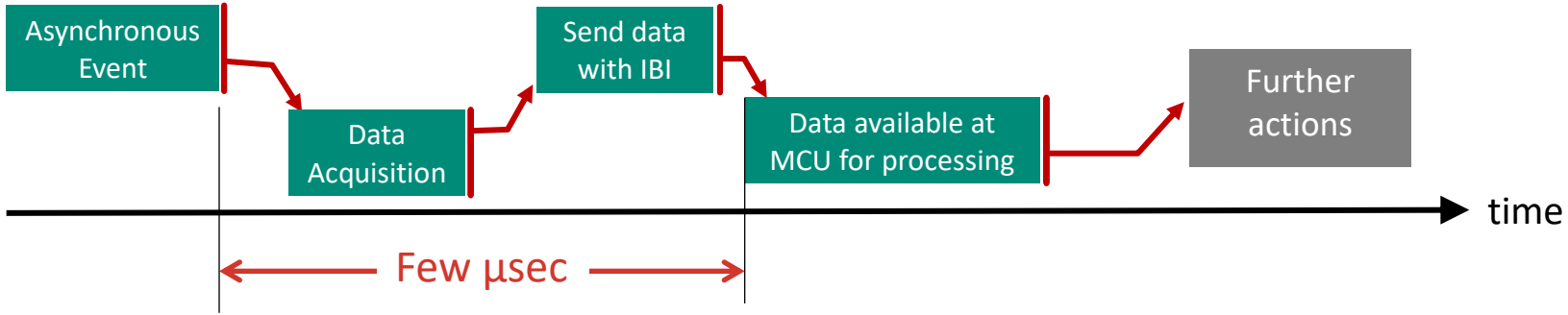
- ENTASx is only a “suggestion” to Target
- ENTASx does not replace application specific/custom power savings agreements

Activity state CCC	Bus Idle time
ENTAS0	1us
ENTAS1	100us
ENTAS2	2ms
ENTAS3	50m

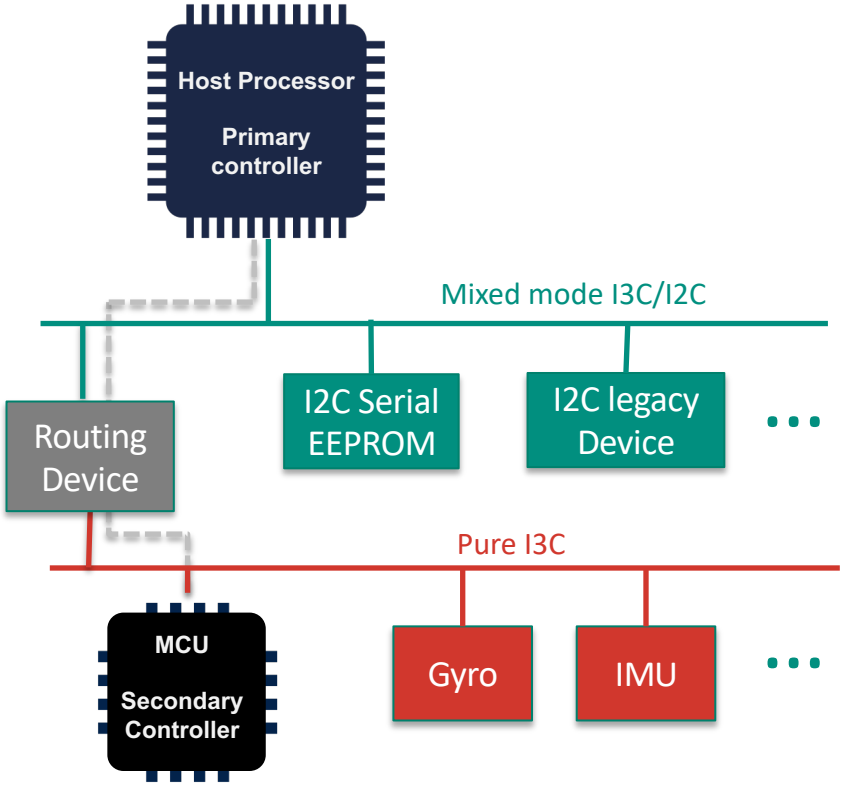
Efficient Data Acquisition with In-Band-Interrupts (IBI)

IBI allows fast and efficient asynch data acquisition, and event processing

- Data produced by a target is promptly transferred to upstream controller for further processing
- IBI intended as an efficient mechanism for Targets to grab Controller attention
- Avoids extra dedicated wires, or inefficient polling mechanism



Improving Bus Activity with Segmentation



Segmentation improves overall system efficiency:

- Isolate high activity (HA) Data producers from low-activity (LA) Targets on a pure I3C Bus segment
- I3C Routing Device bridges Red HA bus from Green LA bus
- Reduced load on Primary Controller MPU

Other Power-Saving Features Enabled by I3C

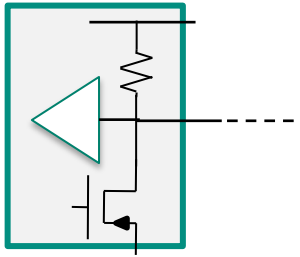
- **Hot-Join**
  - Allow to selectively manage power-on/off of subsystem
- **Device-to-Device Tunneling (D2DT)**
  - Allows direct communication between two Targets, assisted by the Controller
- **Timing Control**
  - Synchronous data acquisition, minimizing uptime of DAQ Target
- **…several others**

I3C Bus Transactions

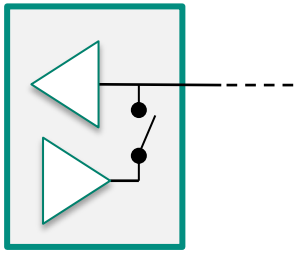
An in-depth look

I3C Bus Electrical States

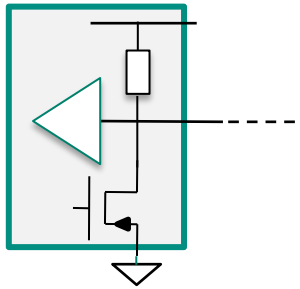
Open Drain (*)
(with Pull-Up)



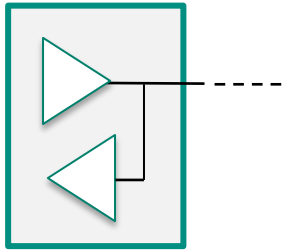
Hi-Z



High Keeper



Push-Pull

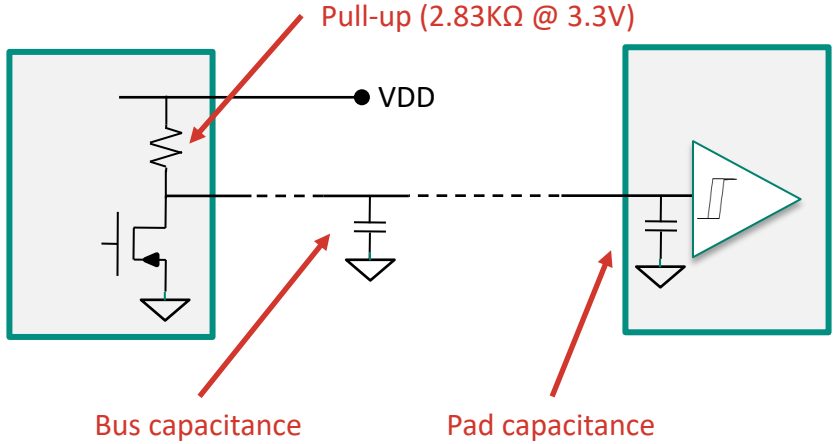


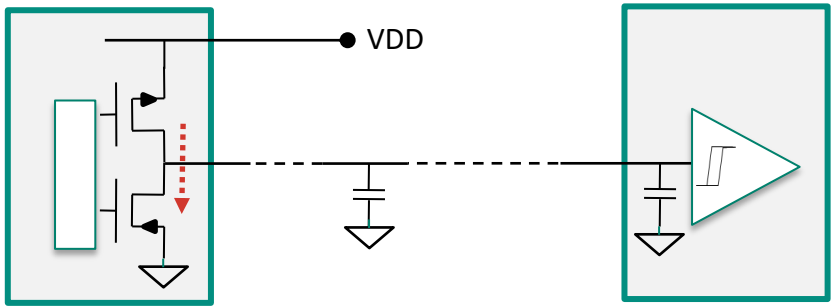
(*) SDA only

- **I3C bus lines can be in four configurations:**
  - Open Drain
  - Push-Pull
  - Hi-Z
  - Hi-Keeper (light pull-up, higher dynamic R)
- **SCL line is (almost) always Push-Pull**
  - No clock stretching
- **SDA is switched dynamically by the Active Controller & Targets between:**
  - Open Drain / Push-Pull / Hi-Z / Hi-Keeper

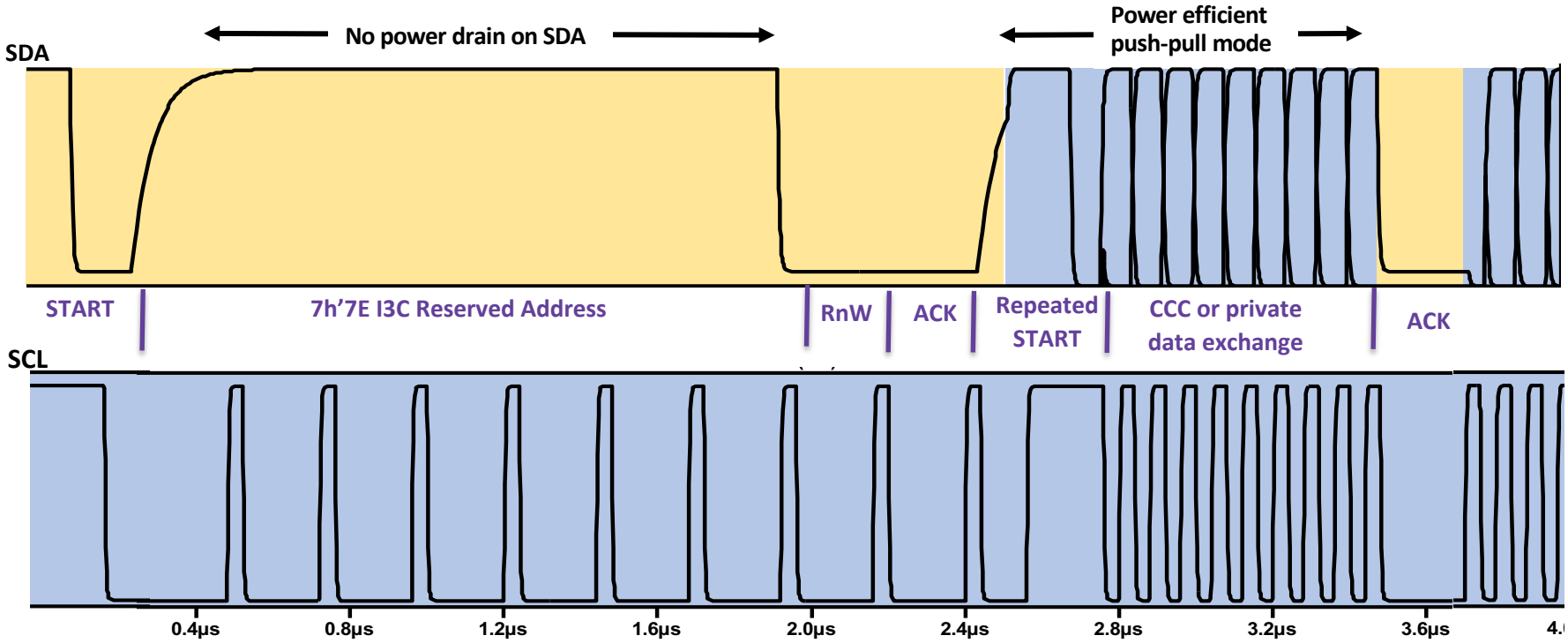
I3C Bus Sources of Power Consumption

- **Electrical**
  - Low Operating voltage: 1.2V - 3.3V
  - Bus capacitance <10pF / device (total 50-100pF)
  - Pull-up: 1.1-2.8 kΩ
- **Factors affecting energy consumption**
  - Open-Drain Pull-down current
    - → Minimize pull-down time
    - → Use push-pull whenever possible
  - Bus capacitance:
    - → Keep short bus length
    - → Reduced Capacitance on input pads
  - Push-Pull Switching shoot-through current
    - → Optimize IP selection





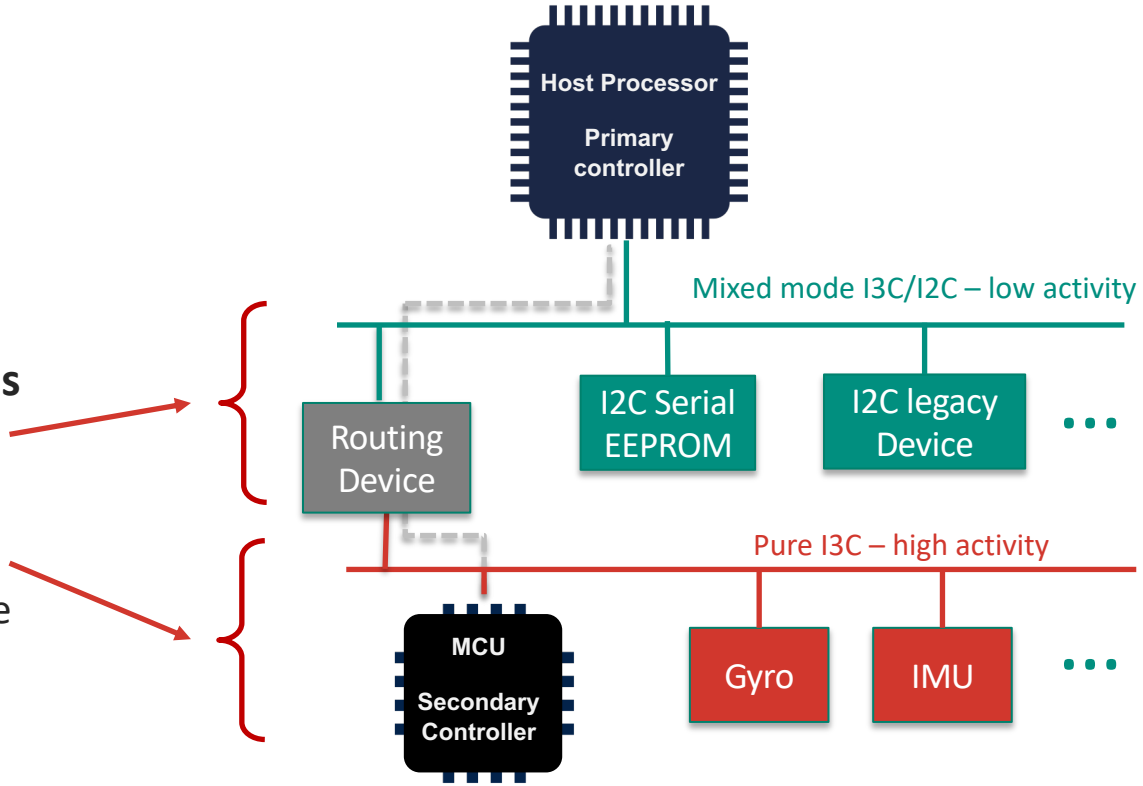
Typical I3C Bus Transaction



Note: There are a few instances where SCL is in Open drain mode, mostly related to I2C compatibility

Optimize by Bus Segmentation

- **Isolate I3C high activity devices**
  - Low activity bus & mixed mode I3C/I2C
  - High activity bus pure I3C, individual targets still accessible
- **Better processing efficiency**

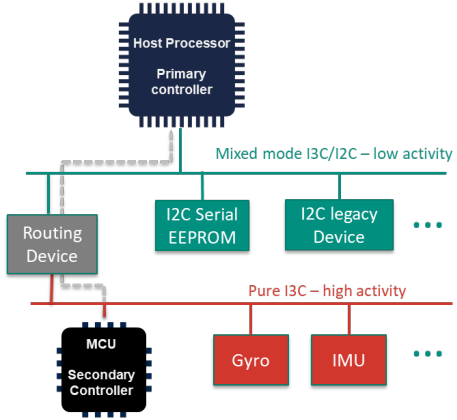


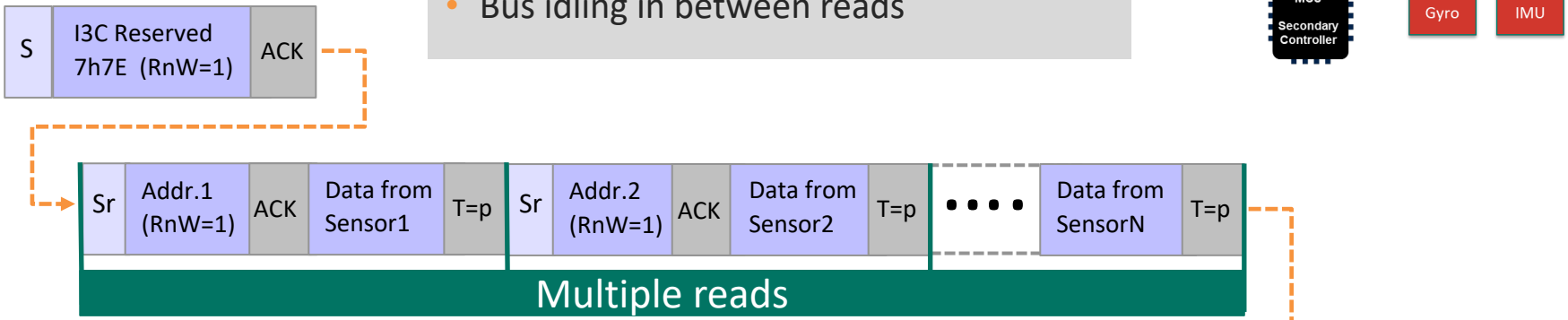
Specs ref. v1.1.1 (5.1.9.3.17/20)

Sequential Operations

Multiple Reads in SDR Mode

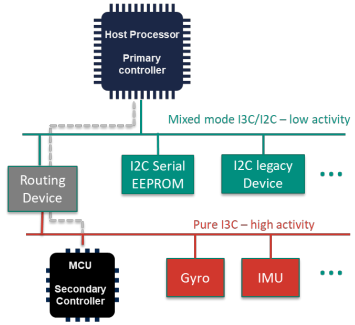
- Suitable for scheduled interrogation
- Bus idling in between reads





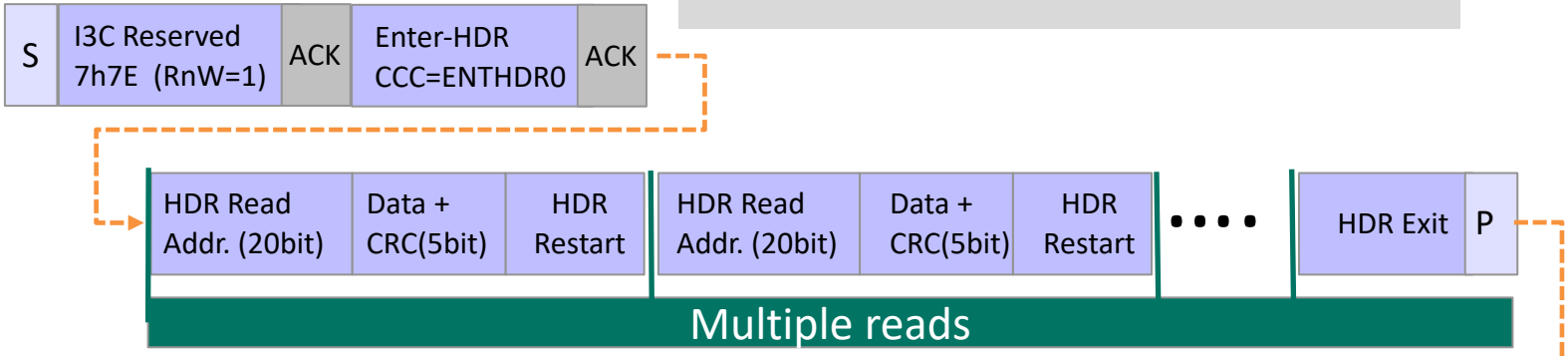
S=START
Sr=START repeated
P=STOP
p=parity bit

Sequential Operations (2)

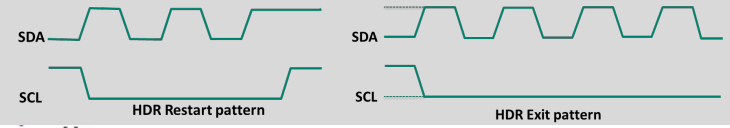


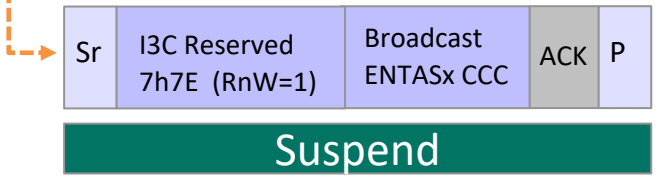
Multiple Reads in HDR-DDR Mode

- Faster read
- Reduction of SCL transition (close to ÷2)
- Data protected by 5-bit CRC

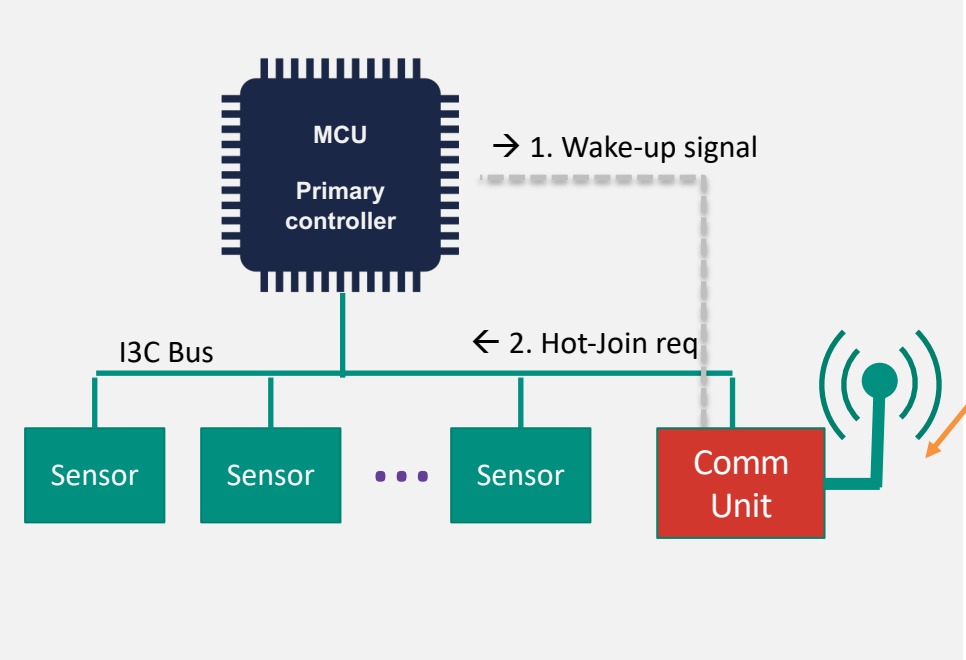


HDR Restart / **HDR Exit** hardware patterns





Power Management with Hot-Join (HJ)



HJ primary use

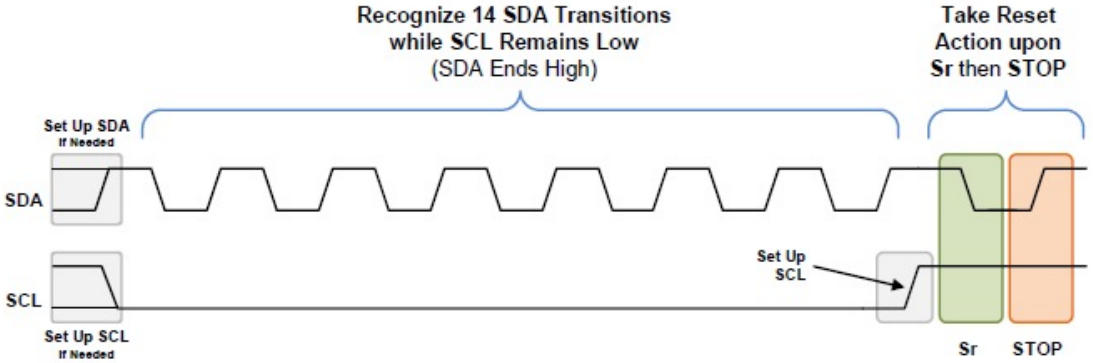
- Attach device after bus is configured
- Provision exist for late power-up of a target

Improved power management

- Selective powering of sub-units
- Wake-up only when needed
- Wake-up signal can be
  - Out-of-band (HW wire)
  - In-band with Target Reset Action (RSTACT) target reacting to a pre-defined pattern

Power Management with Hot-Join

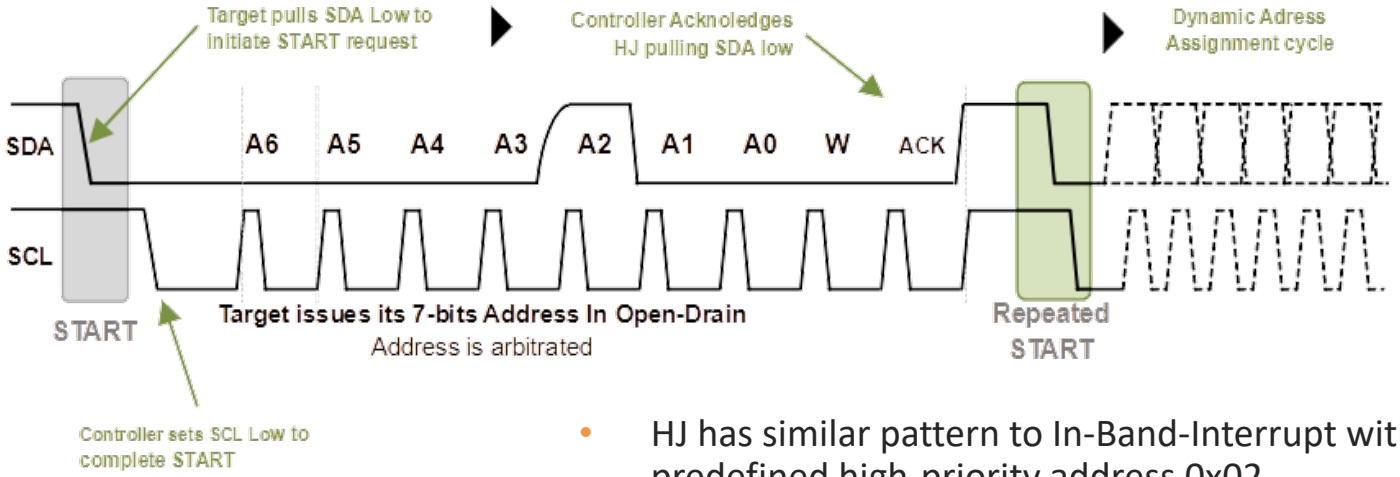
Wake-up with Target-Reset Sequence



- Single HW detection pattern
- Avoids out-of-bus HW and controls
- Multiple wake-up Targets managed thanks to Dynamic Address Assignment during Hot-Join sequence

Power Management with Hot-Join

Joining Sequence



- HJ has similar pattern to In-Band-Interrupt with predefined high-priority address 0x02
- Dynamic Address Assignment need to be executed after x02 Hot-Join opening sequence
- During off-state, target must ensure no power is inadvertently drained thru SDA/SCL wires

Additional Resources

New White Paper

Achieving Power Efficiency in IoT Devices with MIPI I3C

- Introduction to MIPI I3C and I3C Basic Interfaces
- Parameters Affecting Energy Efficiency
- The I3C Electrical Bus
- Optimization by Segmentation
- Improving Idle Time with Bus Conditions
- Efficient Data Acquisition with IBI
- Power Management with Hot-Join
- Efficient Data Transfer with D2DT

resources.mipi.org/download-mipi-whitepaper-power-efficiency-in-iot-with-mipi-i3c

MIPI I3C Additional Information

- **MIPI I3C Specification v1.1.1**
  - https://members.mipi.org/wg/All-Members/document/84923
- **MIPI I3C Basic Specification v1.1.1 Download Page**
  - https://resources.mipi.org/mipi-i3c-basic-download
- **Conformance Test Suite**
  - https://members.mipi.org/wg/All-Members/document/85303 (Member version)
  - https://resources.mipi.org/i3c-test-suite-download (Public version)
- **MIPI I3C Host Controller Interface v1.1**
  - https://www.mipi.org/specifications/i3c-hci
- **MIPI I3C and I3C Basic Frequently Asked Questions**
  - https://www.mipi.org/resources/I3C-frequently-asked-questions
- **MIPI in Internet of Things (IoT)**
  - https://www.mipi.org/internet-things-iot#whitepapers
- **MIPI I3C Basic in JEDEC DDR5: A Sum Greater Than Its Parts**
  - https://resources.mipi.org/blog/mipi-i3c-basic-in-jedec-ddr5-a-sum-greater-than-its-parts

Get Involved / Sources of Further Information

- **I3C Working Group**
  - Open to MIPI Contributor members (meets Wednesdays 08:00 PT)
- **IoT Interest Group**
  - Open to MIPI Contributor & Adopter members (meets 2nd Thursday of the month 08:00 PT)
- **Contact the I3C Working Group and IoT Interest Group**
  - Email: i3c@mipi.org, iot-group@mipi.org (members)
  - Email: admin@mipi.org (non-members)
- **Website:** https://www.mipi.org/specifications/i3c-sensor-specification

Q&A Session

Thanks for attending!