MIPI SPMI System Power Management Interface

v1.00.00 Adopted: 4Q 2008
v2.0 Adopted: Q3 2012

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Specification SPMI

Current Version

- System Power Management Interface v2.0

Primary Use Cases

- Power Management Control Bus
  - Dedicated commands for Reset, Sleep, Shutdown, Wakeup, Authenticate
  - Low latency Register 0 Write command
- General Purpose Multi-master, Multi-slave Read/Write Bus
  - Master-to-Slave, Slave-to-Master, Master-to-Master and Slave-to-Slave Read/Write Commands
  - Burst Read/Write Commands

Specification SPMI

Major Features

- 2-wire, bi-directional interface (SDATA, SCLK)
- Multi-Master, Multi-Slave
  - Up to 4 Masters
  - Up to 16 Slaves
- Request Capable Slaves
  - Able to request arbitration on the bus and send commands
- 2 Speed classifications – SCLK only provided during a transaction
  - Low Speed: 32kHz to 15MHz
  - High Speed: 32kHz to 26MHz
- Master and Slave Arbitration for bus contention resolution
  - Primary and Secondary arbitration priorities for both Masters and Slaves
  - Round Robin priority algorithm for equal access to bus by Masters
  - A-bit and SR-bit arbitration for Slaves
- Slave Group IDs for simultaneous write commands to multiple slaves
- 8-bit or 16-bit address access
- Burst Reads/Writes
  - Up to 16 Bytes with 8-bit addressing
  - Up to 8 Bytes with 16-bit addressing
- Parity bit for error detection (odd parity)
- ACK/NACK on certain commands (SPMI v2.0)

Specification SPMI

Advantages of SPMI

- Replaces point-to-point topology with bus architecture to reduce interfaces and pin counts of SoCs.
- Multi-Master/Slave feature enables Chipset partitioning flexibility for complex and distributed systems.
  - Distributed PMICs (Slaves) for point of load placement
  - Single PMIC (Slave) for reduced part count
- Request Capable Slave messaging reduces side-band signals and pins between Slaves and Masters
- ACK/NACK to confirm correct completion of commands (SPMI v2.0)

Backwards Compatibility

- SPMI v2.0 devices are not compatible with SPMI v1.0 Master and Request Capable Slave (RCS) devices.
- SPMI v2.0 Master devices are compatible with SPMI v1.0 Non-Request Capable Slave (NRCS) devices, if the Master ignores the value present on SDATA during the ACK/NACK cycle.

System Level Integration

- Logical Masters and Slaves may be integrated onto single or multiple physical devices
- Pull down resistor may be integrated into a physical device or on the PCB
- 1.2V and 1.8V signaling voltages defined
- Up to 50pF loading on SDATA and SCLK