mipi alliance

IF IT'S NOT MIPI, IT'S NOT MOBILE

Evolution of MIPI CSI-2 Imaging Conduit

Haran Thanigasalam

Intel Senior Architect | MIPI CWG Chair

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Outline

- MIPI Introduction
- Evolution of MIPI CSI Imaging Conduit
- Q&A

About MIPI Alliance

Peter Lefkin

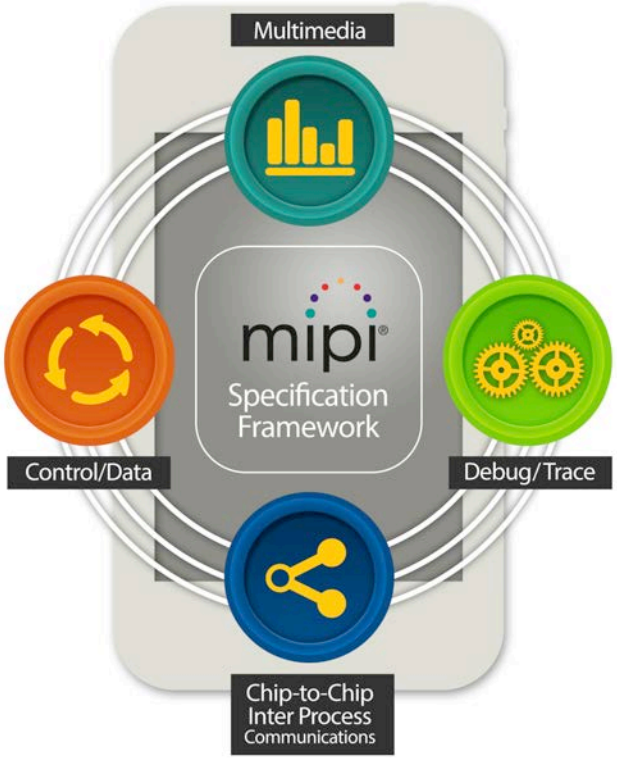
MIPI Alliance Managing Director

About MIPI Alliance

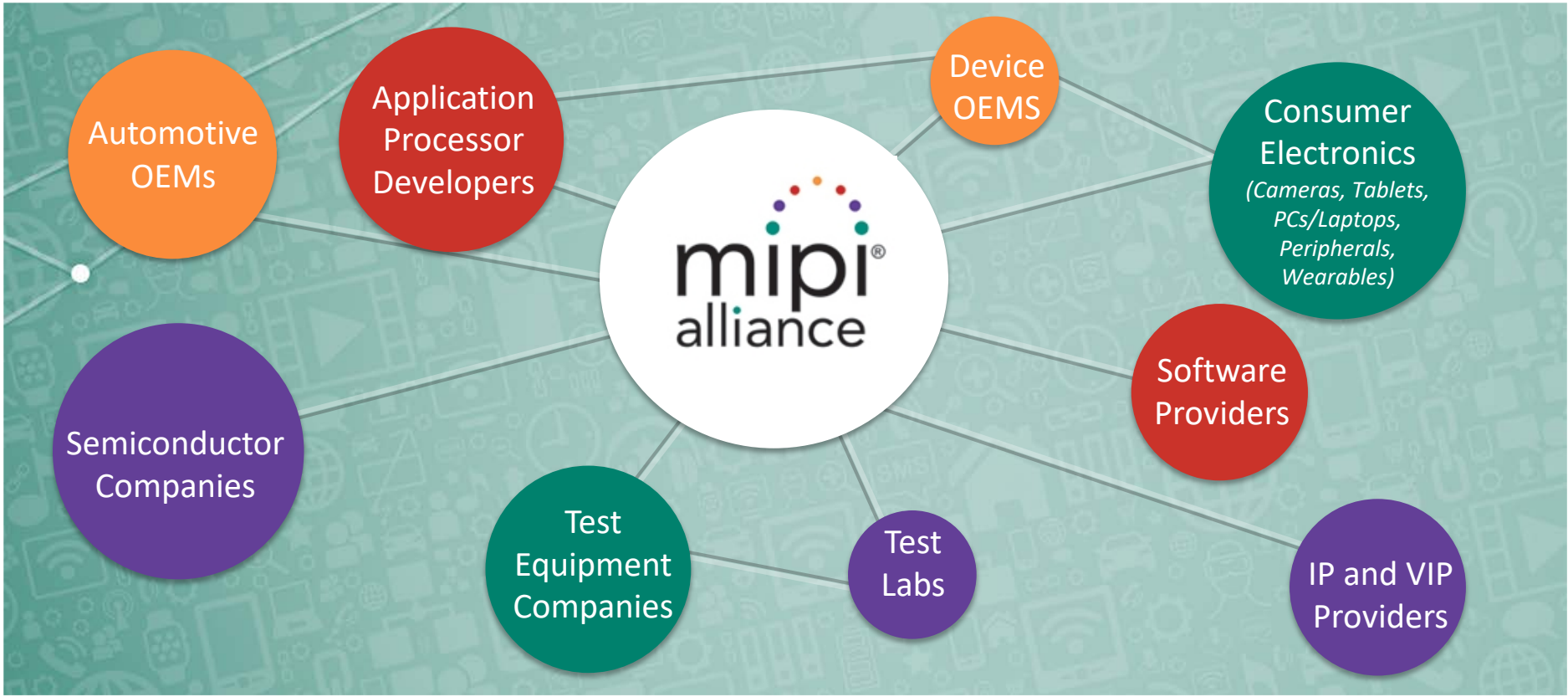
MIPI is a global, collaborative organization founded in 2003 that comprises 300+ member companies spanning the mobile and mobile-influenced ecosystems.

MIPI's mission:

To provide the hardware and software interface specifications device vendors need to create state-of-the-art, innovative mobile-connected devices while accelerating time-to-market and reducing costs



MIPI Alliance Member Ecosystem



What Does MIPI Alliance Do?

Define and promote specifications focusing on the mobile interface but applicable to IoT, auto & more

Provide members with access to licenses as needed to implement and market specified technologies

Complement existing standards bodies through collaboration

Mobile & Mobile-Influenced Markets

MIPI's focus has always been on mobile. In fact, every smartphone on the market today has at least one MIPI specification.

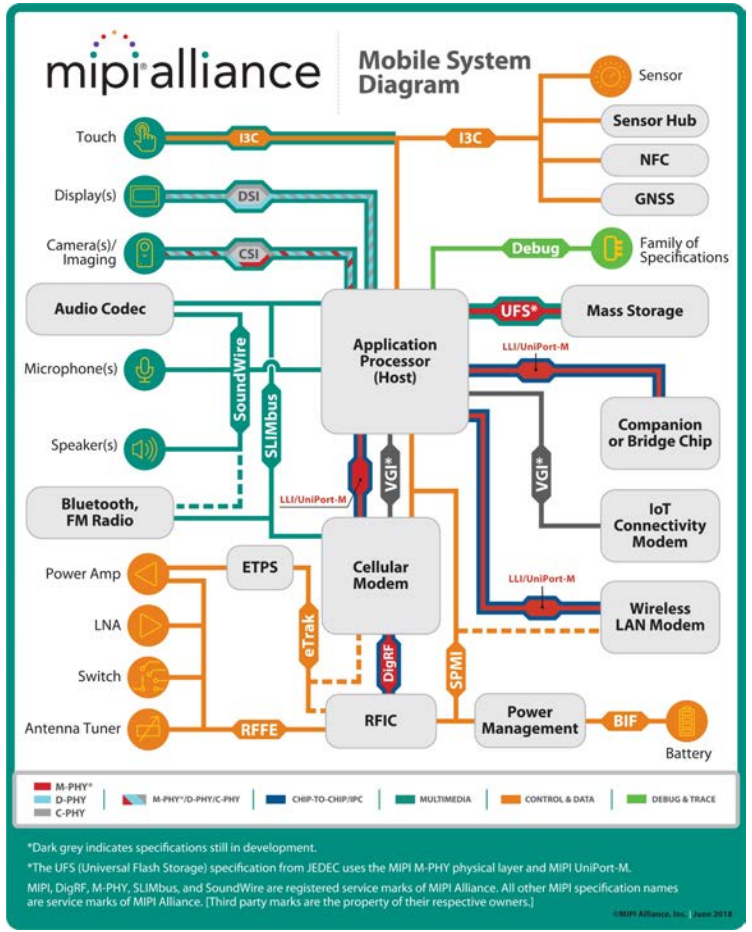
With the development of new mobile-influenced markets, you can now find MIPI specifications in a variety of products:

A System of Mobile Interfaces

To date, MIPI has developed more than **45** specifications. Our leading specifications:

- CSI, CCS
- DSI
- SoundWare
- RFFE
- I3C
- UniPro

Physical layers: C-PHY D-PHY M-PHY



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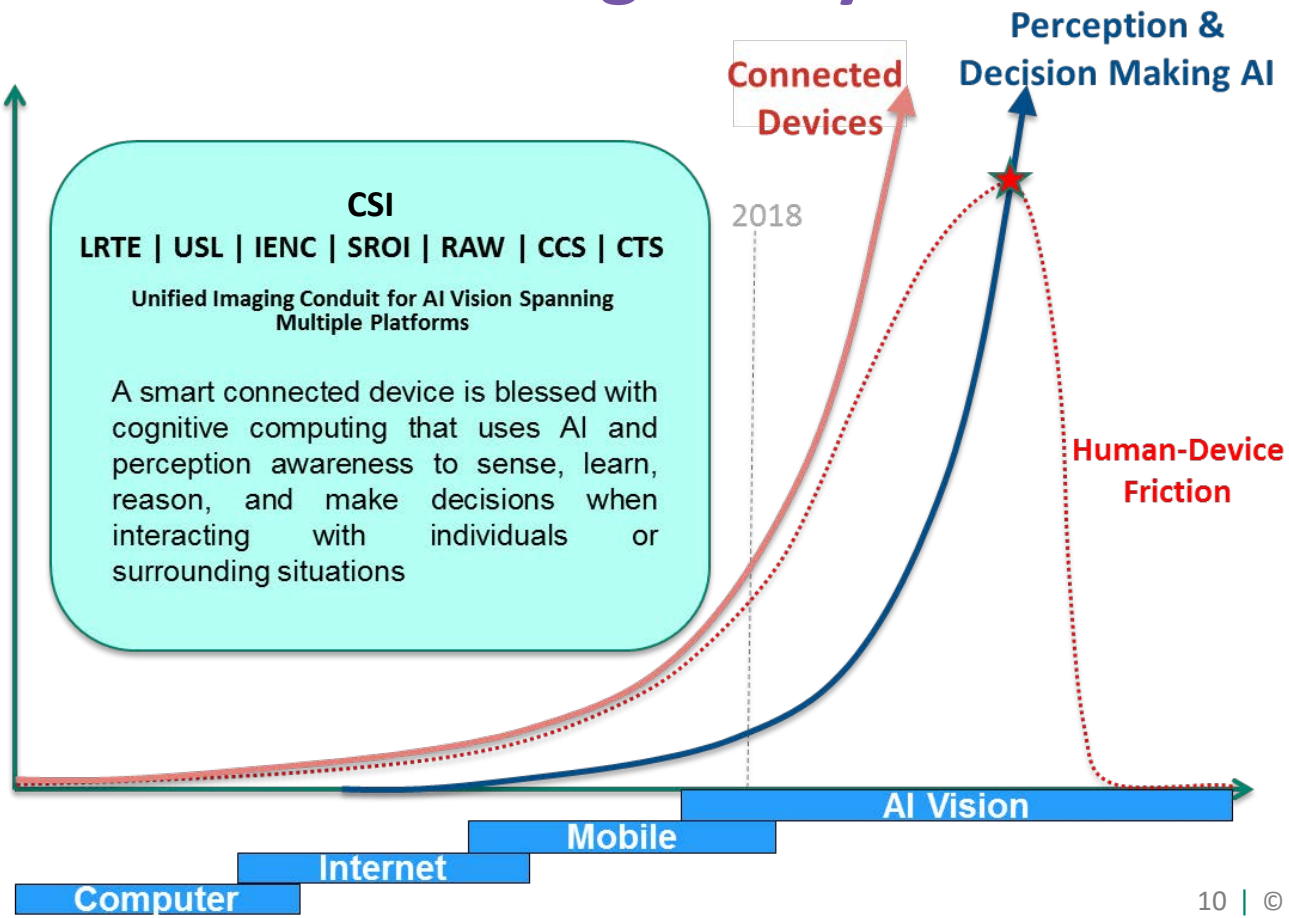
Singularity

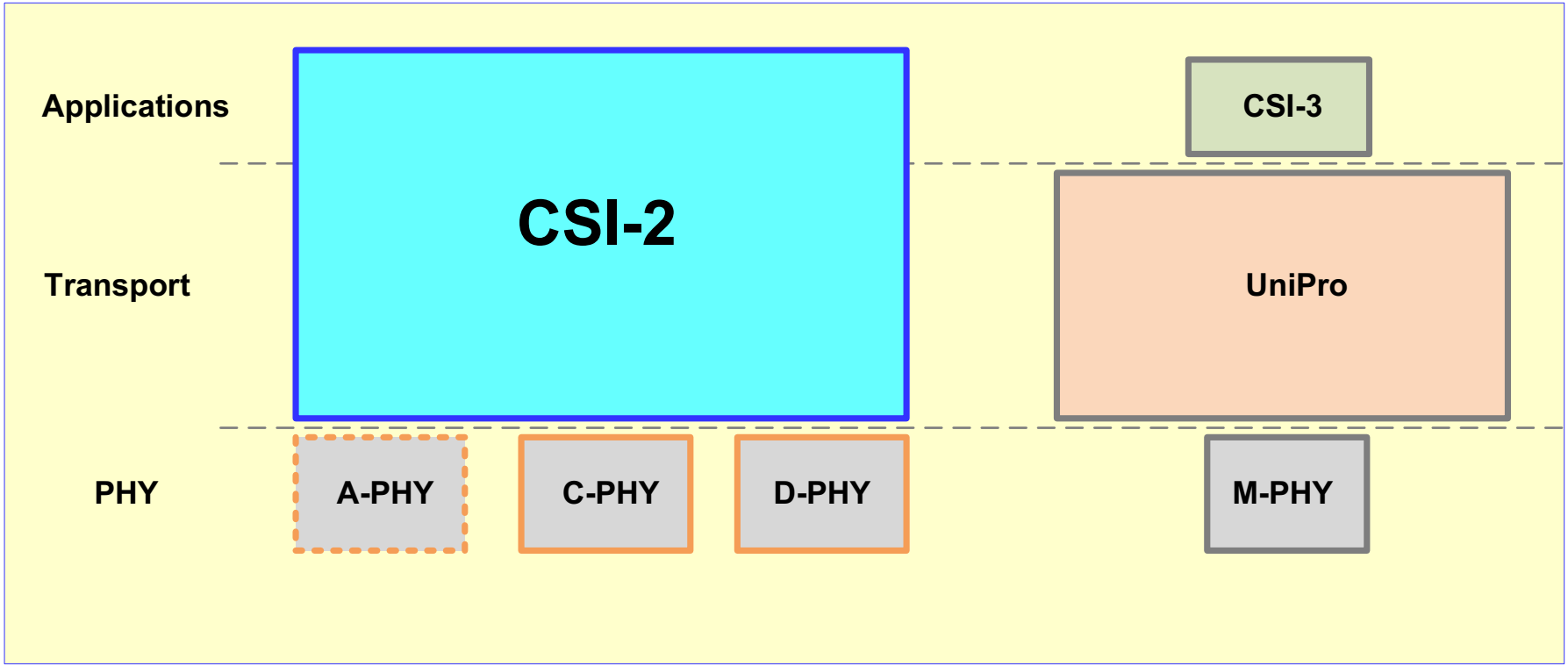


Process

- Use Cases & Applications
- Unified Software Driver
- Features and Capabilities
- End-to-end Conformance Test Suite

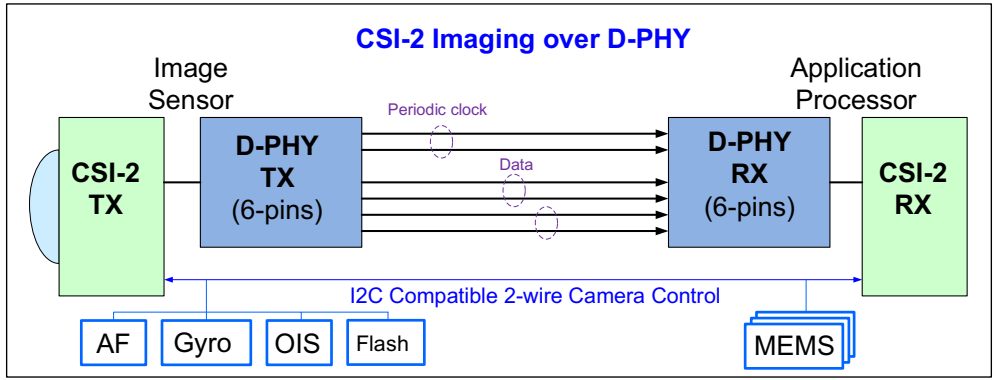
Evolving MIPI CSI

Two different CSI architectures



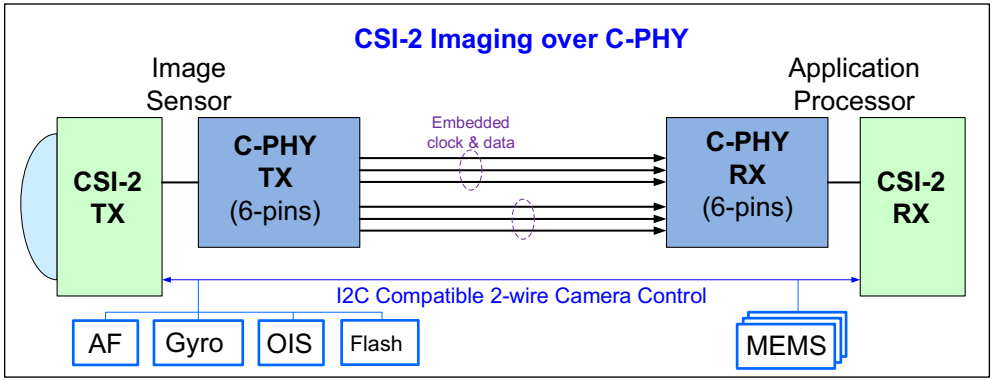
CSI-2 over C/D-PHYs

CSI-2 D-PHY



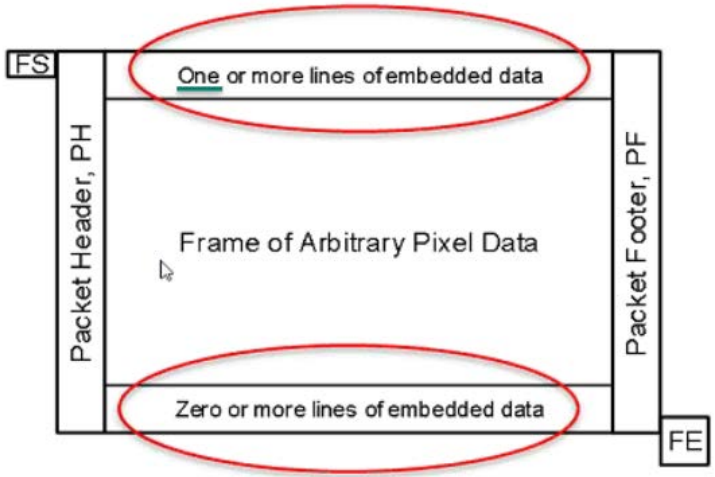
Pin compatible

CSI-2 C-PHY



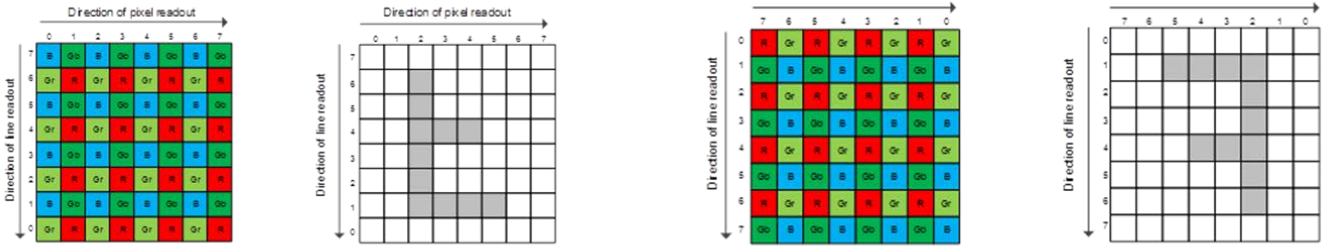
Algorithm is King

- Unified Imaging Software Driver
- Enable Image Sensor Capabilities for Vision Com
- Accelerate Bring up on Reference Platforms

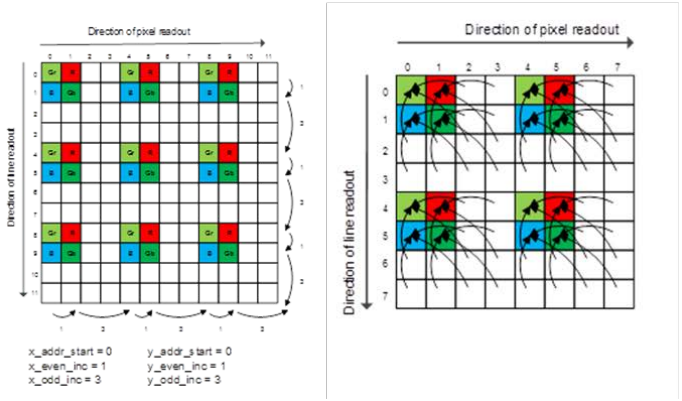


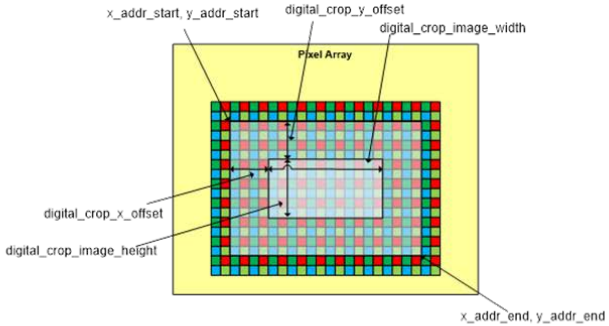
CSI-2 CCS

- Vertical Flip | Horizontal Mirroring



- Sub-Sampled Readout | Binning | Digital Crop



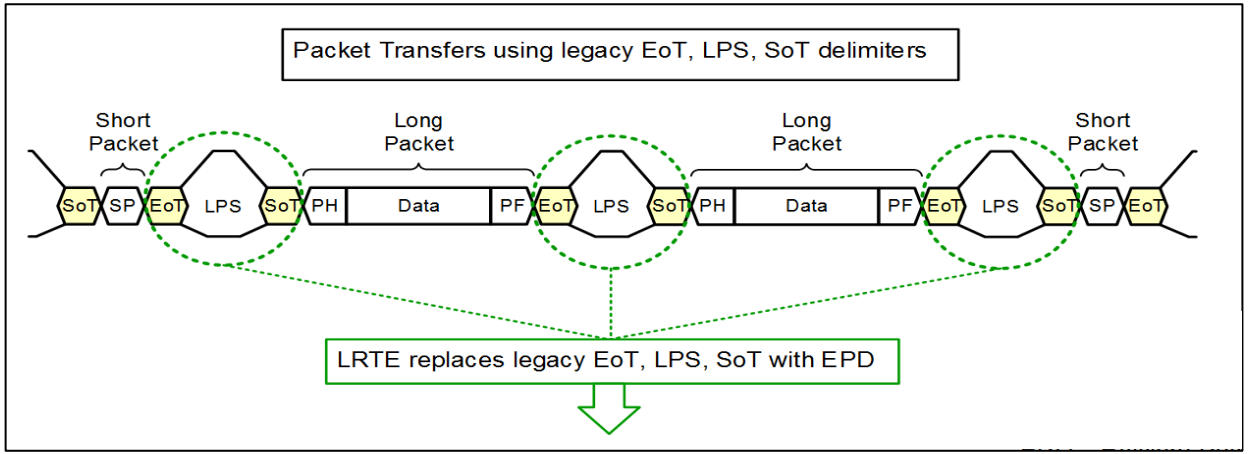


Deep Neural Networks

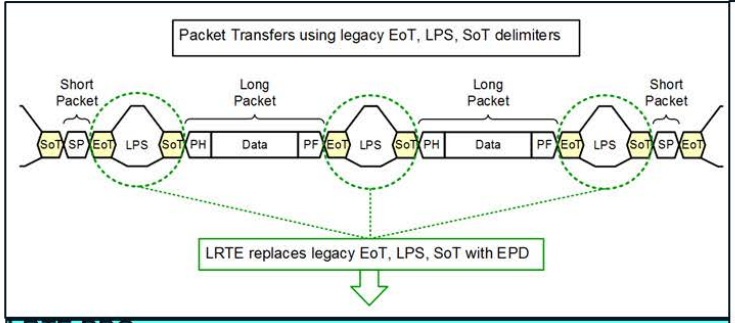
Myriad X Hybrid Arch Deep Neural Network
8 Cameras using 16 MIPI Lanes - 700 MP/s
Drone Collision Avoidance (DJI SPARK)

http://www.electronicdesign.com/industrial-automation/intel-s-myriad-x-vision-chip-incorporates-neural-network

LRTE



- Dramatically Improve Sensor Aggregation
- Optimal Transport Preserving Integrity
- Real-time Perception & Decision Making
- Phase out EOS &IL Impediments



LRTE PDQ

i. Increase number of supported sensors by CSI-2 Aggregators (system cost reduction)

ii. Facilitates optimal transport, while preserving CSI-2 packet delimiter integrity

iii. Reduce frame latency for real-time perception & decision making applications

LRTE ALPS (requires PDQ)

Transitionary pathway to phase out (1.2v) EOS impediments

Detailed CSI-2 System Analysis & Benefits of Using LRTE PDQ

System 1: CSI-2 v2.0 over C-PHY v1.2 (3.5 Gsps/lane or 8Gbps/lane)
- 24 Gbps using 3 lanes (requires 9 wires)
- CSI-2 v2.0 supports up to 32 Virtual Channels over C-PHY

Multi Sensor Aggregator with each sensor configured as
- 1920 x 1200 (2.3MP), 12 BPP, 60 FPS

Image Sensor Packet Transport
- 1920 pixels x 12bps = 23040 bits per Horizontal Row Long Packet (LP)
- 23040 bits / 24Gbps = 0.960 us / LP (CSI-2 Payload; ignoring PH/PF)
- Packet Header + Packet Footer = 336+48= 384 bits
- 23424bits / 24Gbps = 0.976us /LP_PHF (CSI-2 Payload with PH and PF)

CSI-2 v2.0 with Legacy C-PHY Packet Delimiters:
- LP Delimiter (SoT/EoT) = ~0.3 us
- Total Time per LP_PHF = 1.276 us
- Packet Delimiter Overhead = 23.5%
- Time per Image Frame = 1.276 us x 1200 = 1.53 ms (Ignoring FS/FE)
- Stream 60 frames from single image sensor requires: 1.53ms x 60 = 91.87 ms
- Maximum Supported Image Sensors on an Aggregator = 10
- FLOOR[1/0.09187] = FLOOR[10.88]

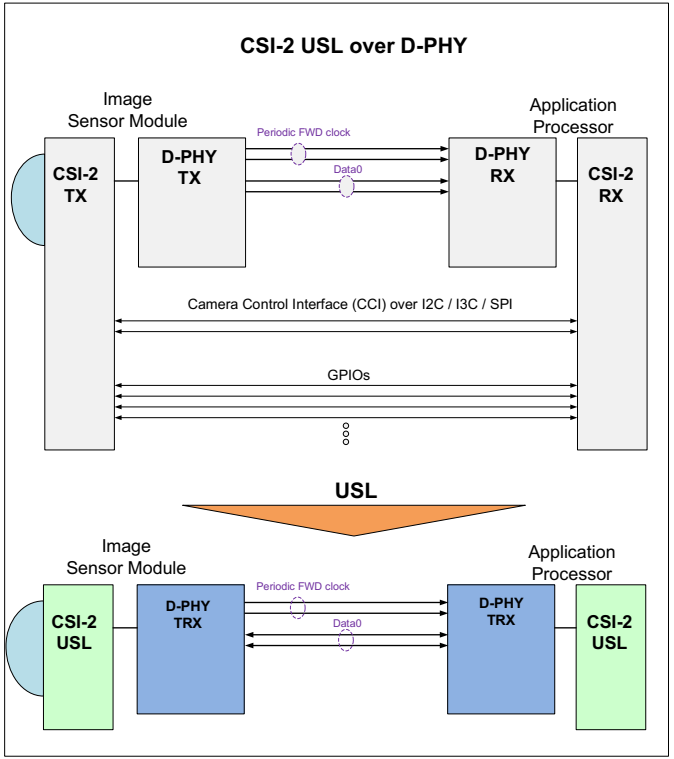
CSI-2 v2.0 with LRTE PDQ:
- Time per Image Frame = 0.976 us x 1200 = 1.171 ms
- Stream 60 frames from single image sensor requires: 1.172ms x 60 = 70.27 ms
- Maximum Supported Image Sensors on an Aggregator = 14
- FLOOR[1/0.07027] = FLOOR[14.23]

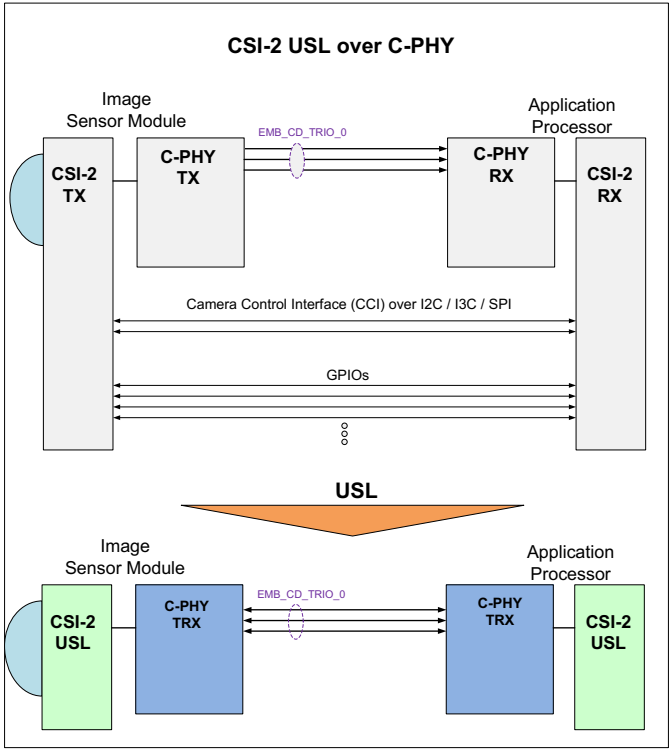
Benefits of CSI-2 v2.0 with LRTE PDQ:
- Frame Transport Efficiency Improvement: 23.5%
- Additional Supported Image Sensors on Aggregator: +4 (over the same channel)
- Alternatively, reduce toggle rate / wires

Considerations	
Legacy PD Hor Row Overhead	23.51%
Legacy PD Max Supported Sesnors	10
LRTE PDQ Hor Row Overhead	0.20%
LRTE PDQ Frame Transport Efficieny Impact (reduce: power / wire / toggle)	**23.35%**
LRTE PDQ Max Sesnors Supported	14
LRTE PDQ Additional Supported Sensors	**40.00%**

USL

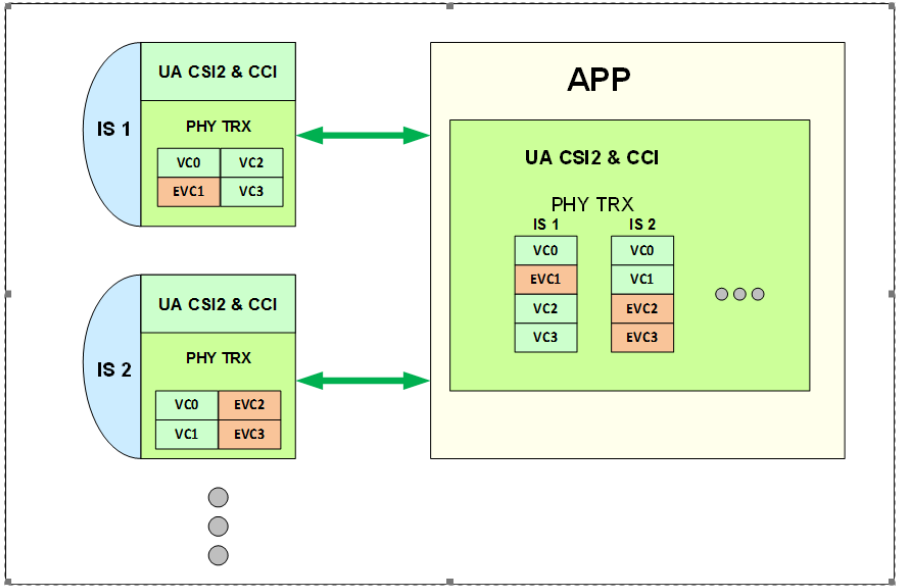
- Long Reach
- Wire Reduction
- Encapsulation
- Secure Channel





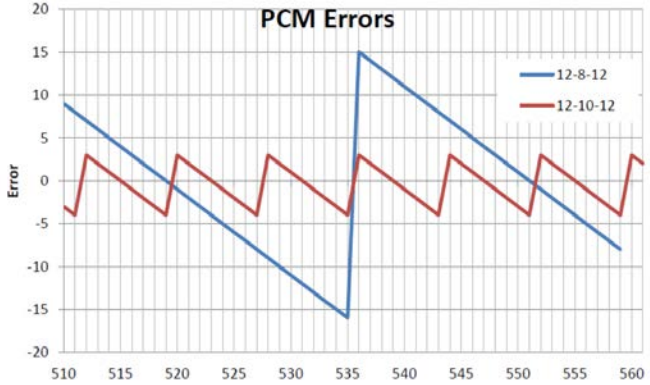
IENC

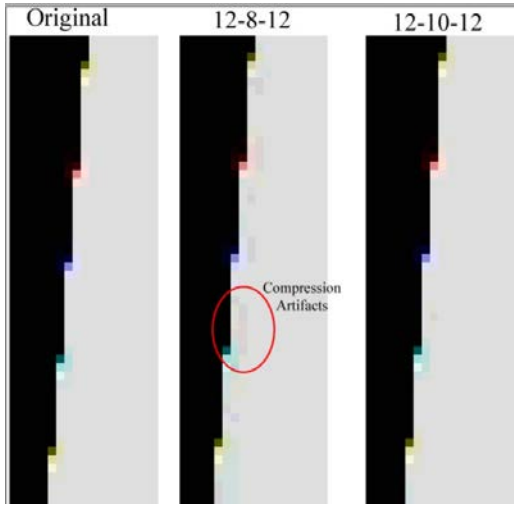
- Enterprise Security
- Pixel Authentication
- VC Mapped Interleaved Encryption
- Threat Model & Use Cases (GCM / AES)



DPCM Objective Qualification

- Enable 10-bit compression of RAW-12 video image with better IQ than prior version 12-8-12
- Reduce maximum absolute error of single-bit change in pixel value by a factor of 4.43x
- Qualified 5 degree slanted edge input image with low, medium, and high illumination levels:
  - 12-10-12 virtually indistinguishable from original image
  - MTF frequency response analysis closely tracks the original (HI/MI/LI - LC/MC/HC)
- Benefits include Link BW reduction cost savings

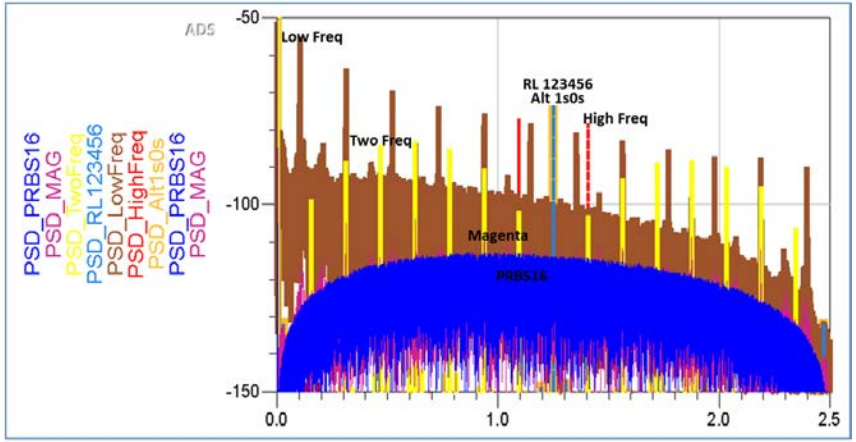




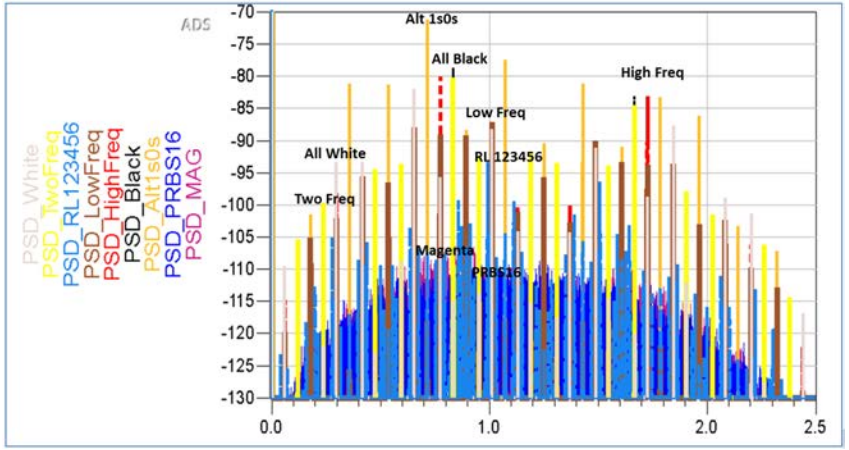
Use Case	Per-Lane 4-Lane Bit Rate (Gbps)				12-10-12 DPCM Enables Use of:
	10 bpp	D-PHY	12 bpp	D-PHY	
4Kp60 or 1080p240	1.485	v1.1	1.782	v1.2	D-PHY v1.1
16M (4:3) @ 30 fps	1.45	v1.1	1.74	v1.2	D-PHY v1.1
20M (16:9 crop) @ 30 fps	1.371	v1.1	1.645	v1.2	D-PHY v1.1
32M (4:3) @ 24 fps	2.263	v1.2	2.715	v2.0	D-PHY v1.2

PSD Reduction

CSI-2 over D-PHY PSD emission reduction with scrambling (data lanes)



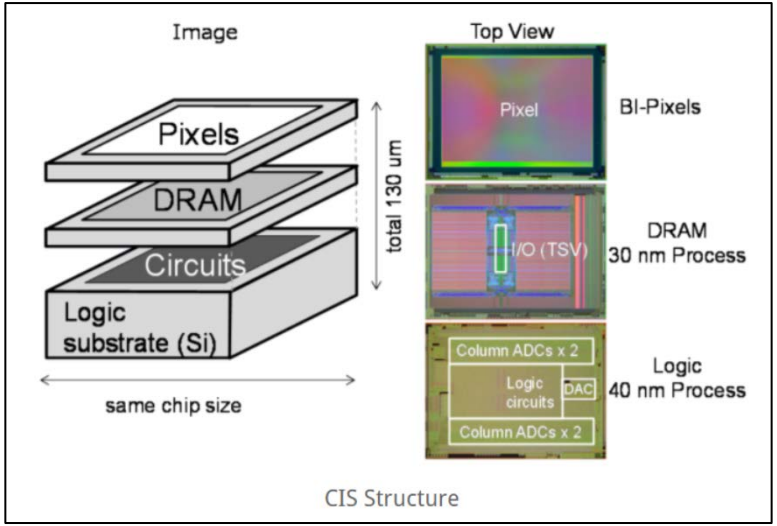
CSI-2 over C-PHY PSD emission reduction with scrambling (embedded clock and data)



SROI

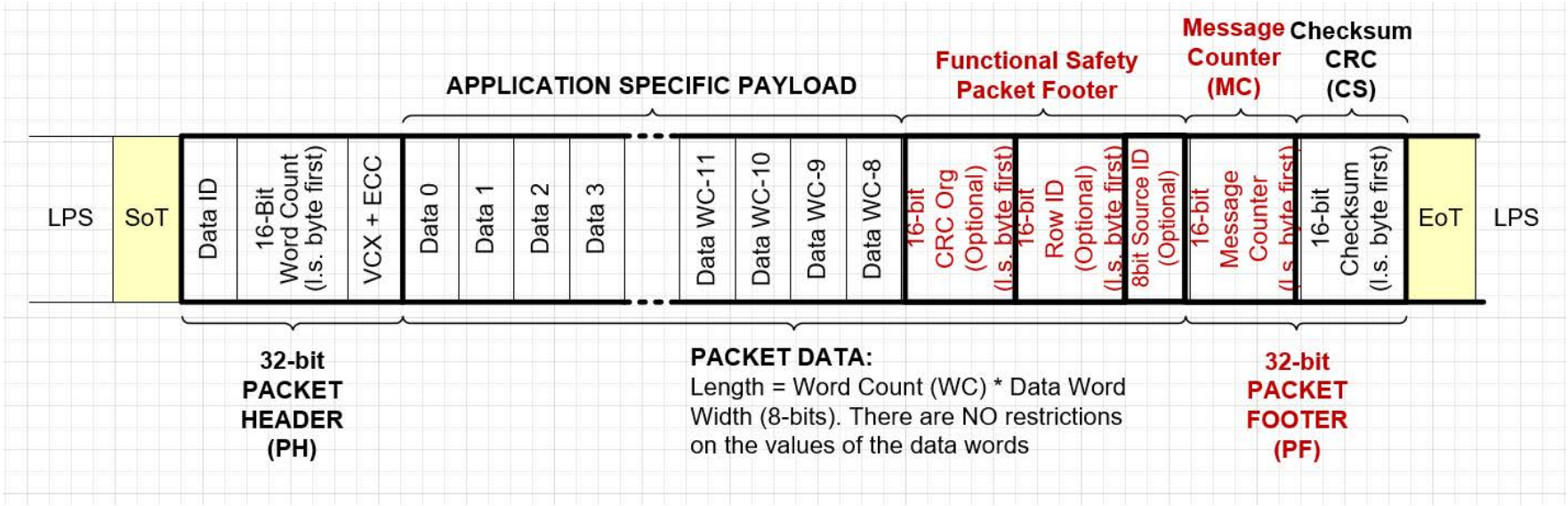
- Phase 1 EOY 2018 Single Frame
- Phase 2 EOY 2019 Multi Frame
- ARCH: Central | Edge | Hybrid

3-layer stacked image sensor

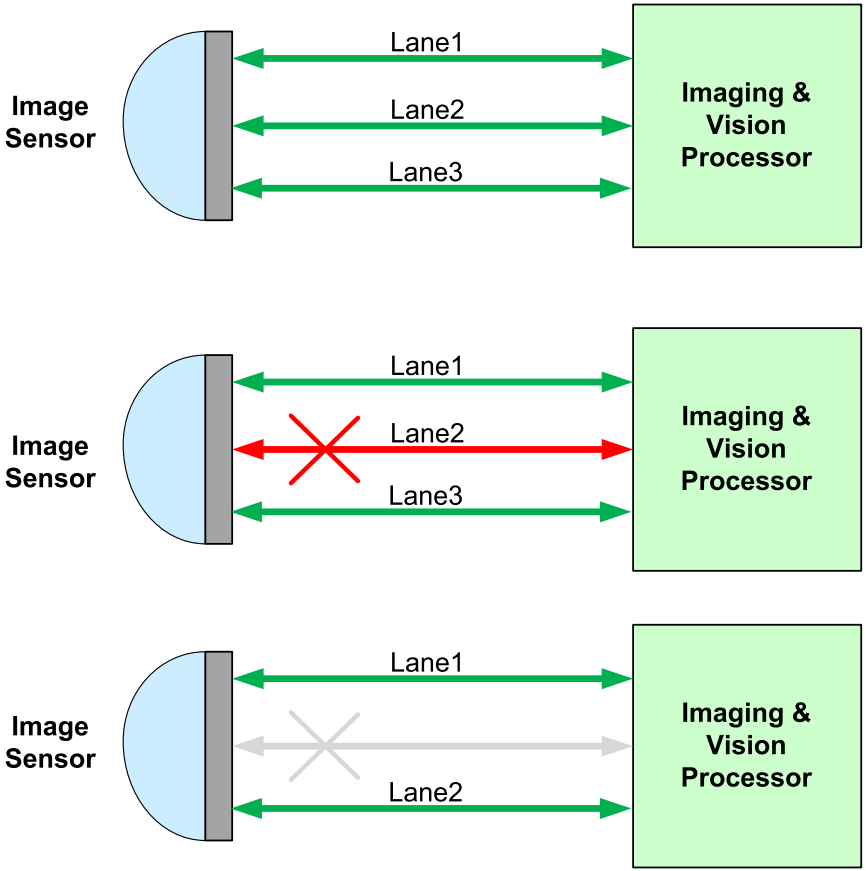


https://fuse.wikichip.org/news/763/iedm-2017-sonys-3-layer-stacked-cmos-image-sensor-technology/

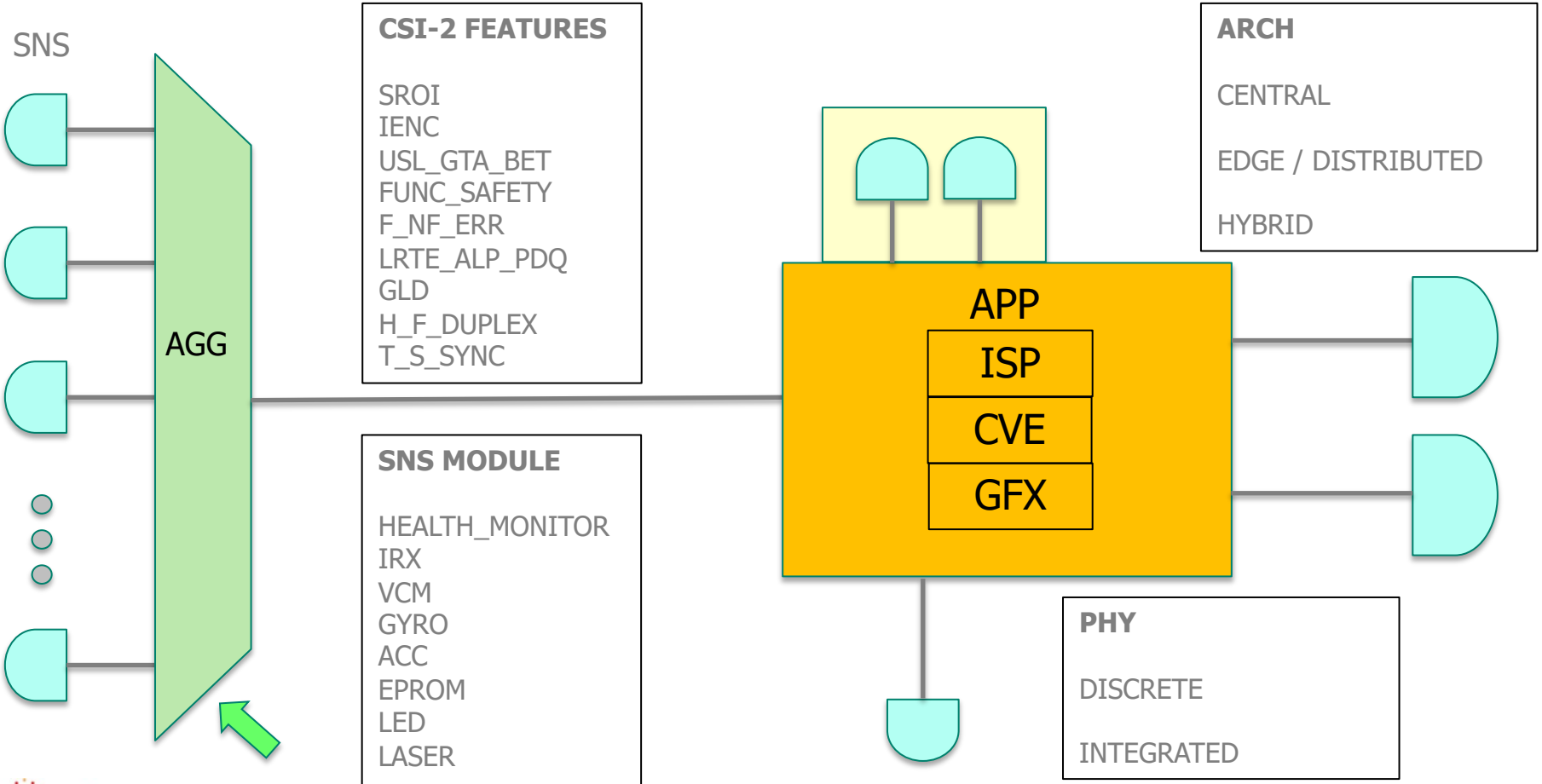
Functional Safety



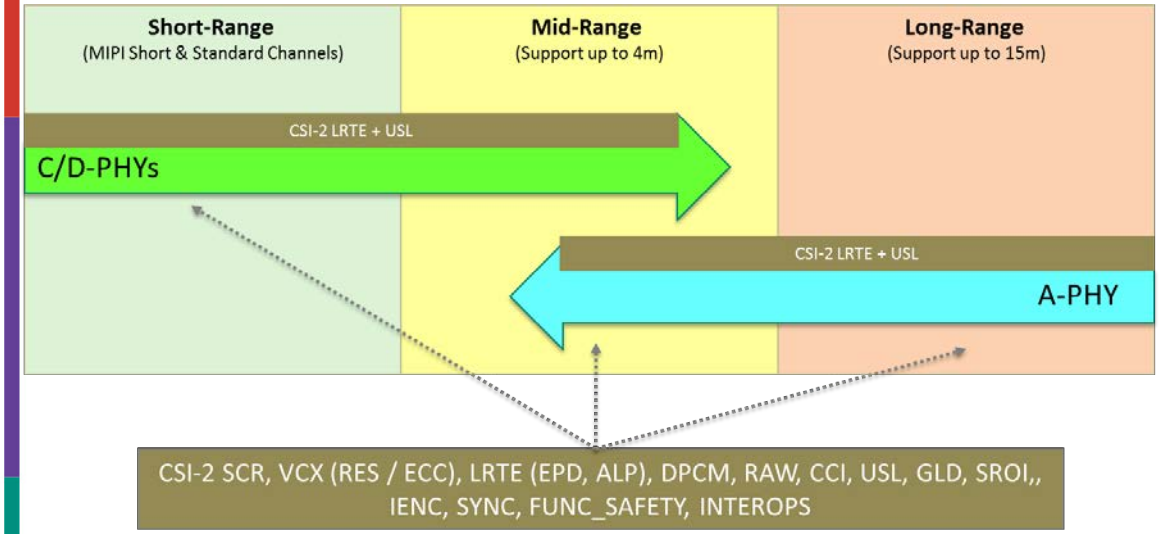
Graceful Link Degradation

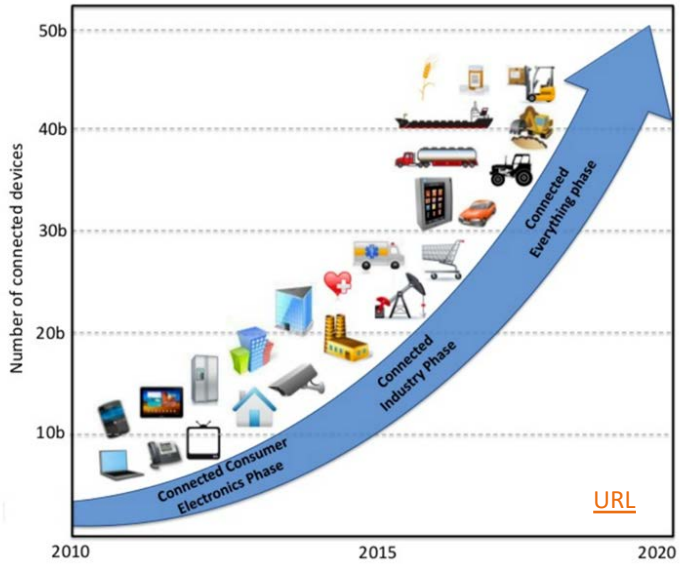


End-To-End Imaging Conduit



Interconnect





- Mid-Range solutions targeting Seoul FTF

Topology

Form Factor	Mobile	Phablet	Tablet	2:1	Notebook (Hinge)	AIO / IOT	Panel	AR/VR	Drones (Commercial)	Robotics & Medical
Reach	4”	6”	8”	12”	15”	30”	40”	60”	24”	60”
Cable	Flex	Flex	Flex	STP	UTP (thin) Flat behind / round edge	STP	STP	STP	Flex (lower weight)	STP
USL	Optional	Optional	Optional	Optional	Yes	Yes	Yes	Yes	Yes	Yes
SCR / SSC*	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
D-PHY*	1080p, 10 BPP, 30 FPS using 1 Lane / 4 wires / 0.69 Gbps (SSC recommended for D-PHY FWD Periodic Clock)									
C-PHY	1080p, 10 BPP, 30 FPS using 1 Trio / 3 wires / 0.30 GSps									
A-PHY	N/A	N/A	N/A	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Topology	FR4-FLEX-FR4	FR4-FLEX-FR4	FR4-FLEX-FR4	FR4-STP-FR4	FR4-FLEX-STP-FR4	FR4-STP-FR4	FR4-STP-FR4	FR4-STP-FR4	FR4-STP-FR4	FR4-STP-FR4
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Summary

- CSI-2 imaging features mapped to AI & vision
- Unified imaging SW driver
- Comprehensive ETE Conformance Test Suite
- Natively support short / mid / long range platforms
- Solutions targeting IoT platforms at the Seoul FTF

Questions

https://mipi.org/working-groups/camera