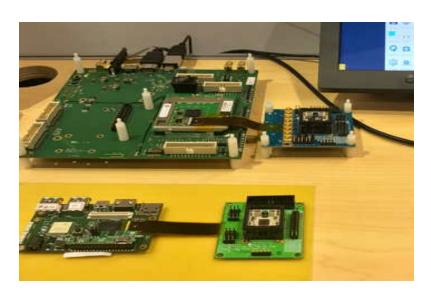
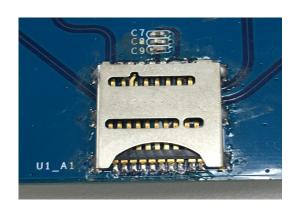


M-PHY Gear 4 Test Challenges

Very hard to debug interoperability issues at this moment

- No Gear 4 protocol analyzer available (schedule available at end of 2017)
- > Hard to measure or probe 12Gbps signal quality in embedded or even a UFS card connector
- > Tx/Rx Instruments cost are very high
- > Signal quality uncertain after CTLE+DFE equalizer circuit
- > Due to these issues, need to try and error when system is not working. Schedule impact





Not Easy





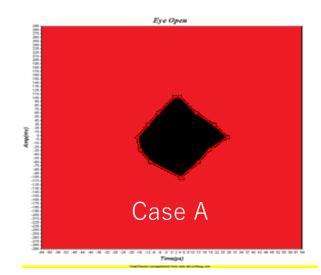
In Order to Understand Receiver Quality - 1

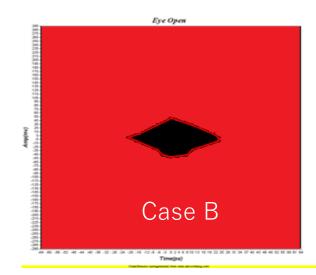
Solution 1: Eye Open

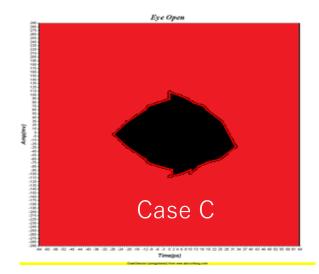
Pro: 1) Know if Rx sees data stable window

2) Easier to implement circuit

Con: No idea about signal quality information







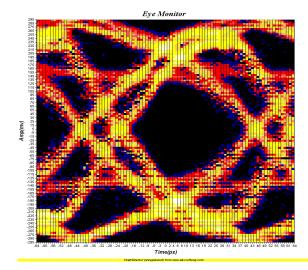


In Order to Understand Receiver Quality - 2

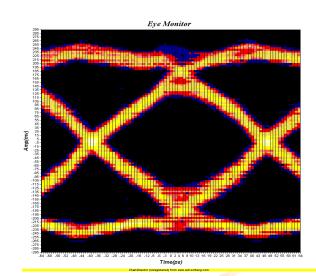
Solution 2: Eye Monitor ON THE FLY

- Pro: 1) Detailed information about signal quality available
 - 2) Is there reflection? Too much loss or too much compensation
 - 3) User can provide eye monitor for debugging

Con: More complicated circuit design



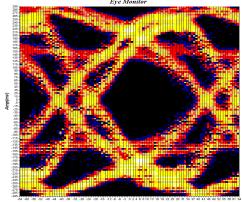
Guess Case A or B?

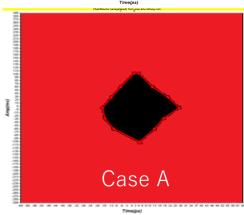




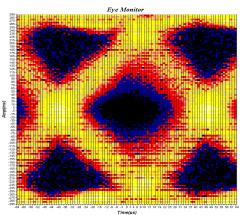
Eye Open vs Eye Monitor

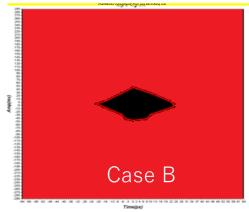
Too Much Compensation



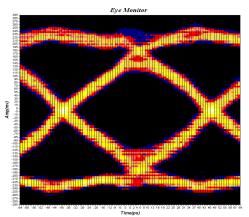


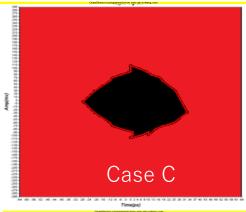
Need More Compensation





Nice One!

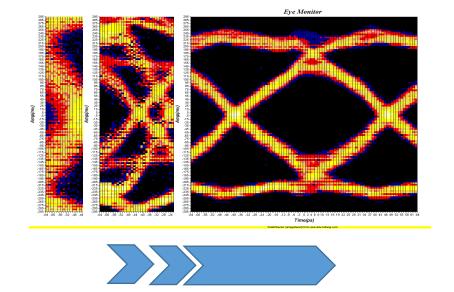






And More.... Getting Best Cal Setting in Embedded System

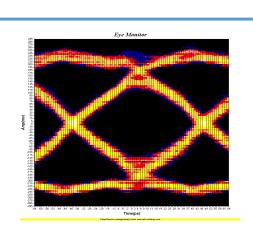
With Eye Monitor function + post processing algorithms, each chip is able to select the best eye monitor result in the specific embedded system as its default parameter







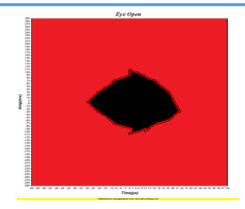
Eye Open vs Monitor Comparison Table



Operation Timing

- ➤ Take fewer seconds for the detailed eye
- Adjustable scan timing setting

- Signal Quality Info
- Great signal quality information
- Good for debugging

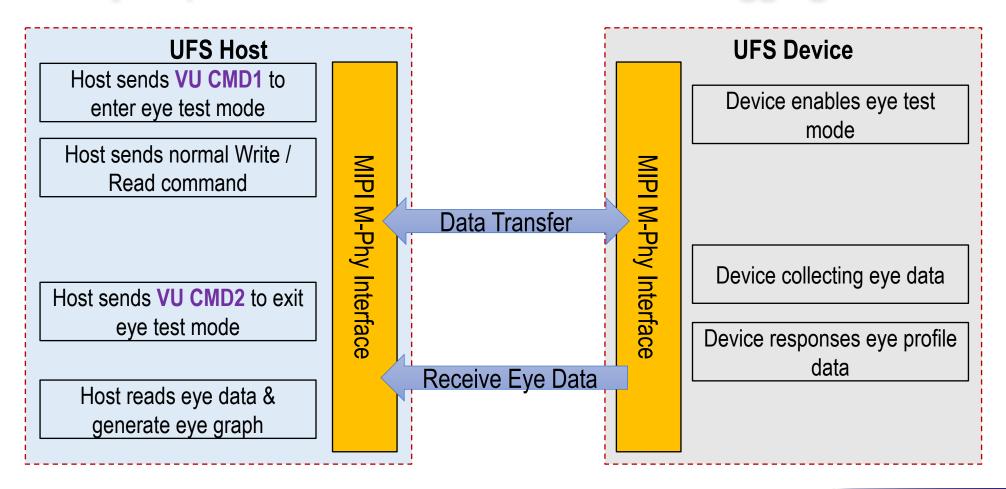


- > Fast
- Possible done within Gear 4 ADAPT package (EQ tuning)

See data stable window only

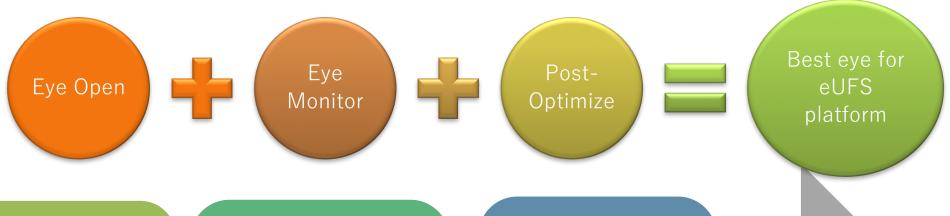


How Eye Open/Monitor Works for UFS Debugging





Best Eye Result for Embedded UFS Platform



Eye Open

- Fast operating timing
- Apply during ADAPT

Eye Monitor

- Good signal quality information
- Extract best setting during eUFS shipping

Post-optimization processing

 Select the best eye monitor result in specific embedded system

Best Interoperability

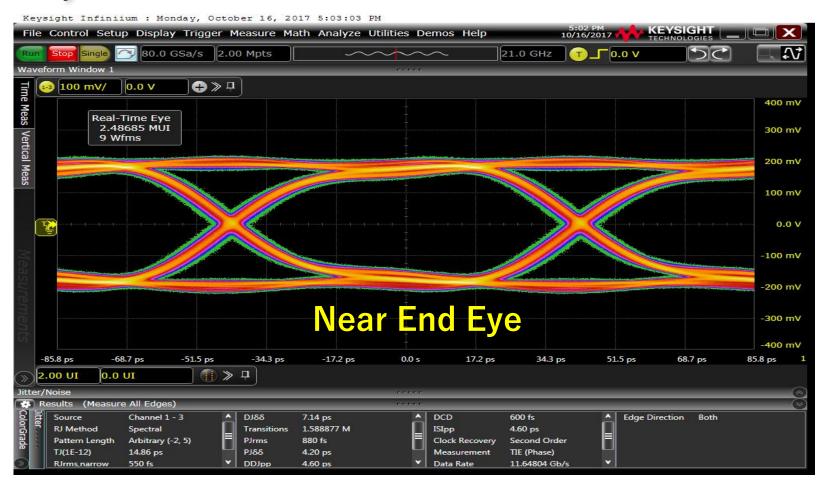


Phison Gear 4 Performance

- ✓ Power consumption : < 5mW /Lane/Gbps (28nm)</p>
- ✓ Support HS-MODE Gear4(A/B) with data rate up to 11.6 Gbps and backward compatible
- ✓ Support for 2-lane M-TX and 2-lane M-RX
- ✓ Supports LS-MODE PWM-G1 to PWM-G4 with data rate up to 72 Mbps
- ✓ Supports Type-I MODULE state machine for HS and LS mode
- ✓ RMMI M-RX/TX-DATA interface 40 bit for protocol layer data interface



G4B Tx Eye Results





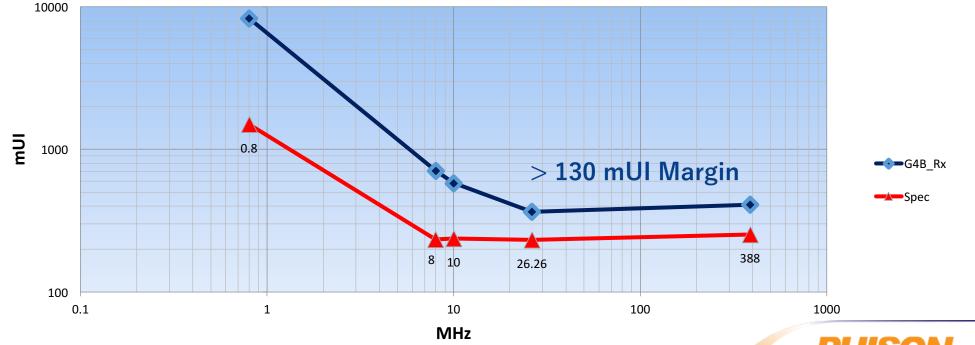
G4B 11.648Gbps Rx Compliance Margin Results







MPHY_2.45_Beta18







PS8313 UFS Storage

- eUFS 2.1, Gear 3, 2 Lanes
- 256GB 3D Nand Flash/LDPC
- Max. R 920MB/s; W 550MB/s



M-PHY Gear4 IP

- Compliant with M-PHY 4.1
- Receiver Eye open feature (Test Mode)
- 11.6 Gbps, 2 Lanes



UFS Host Board

- USB 3.0 Device
- Support UFS 2.1 Gear3, 2 Lanes
- Built-in Data Pattern Generator

NAND Flash-based IC Design

Over 15 years of NAND Flash Controller Experience

▶ 1100+ flash related Patents, Internal Phy, ASIC, and Advanced NAND Handling Technologies

System Integration

Broad Application Expertise

- ▶ from Embedded, Enterprise to PC & Mobile
- ▶ from PATA, SATA, NVMe PCIe, USB, SD, eMMC to UFS

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