mipi®
DEVCON

Prem Arora
Microsemi Corporation

Multiple MIPI CSI-2SM Camera Solution Using FPGAs

2017
MIPI ALLIANCE
DEVELOPERS
CONFERENCE

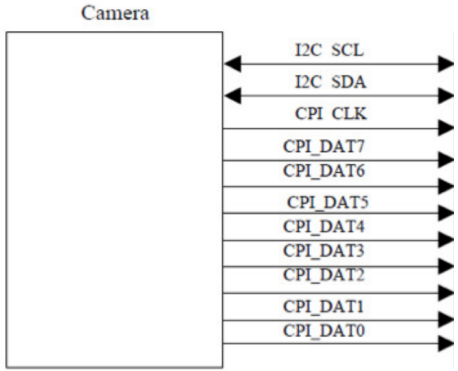
BANGALORE, INDIA
MIPI.ORG/DEVCON

Agenda

- History & adoption of MIPI CSI-2℠ image sensors
- FPGAs in Imaging/Video applications
- Applications for multiple MIPI CSI-2 image sensors with FPGAs
- Summary

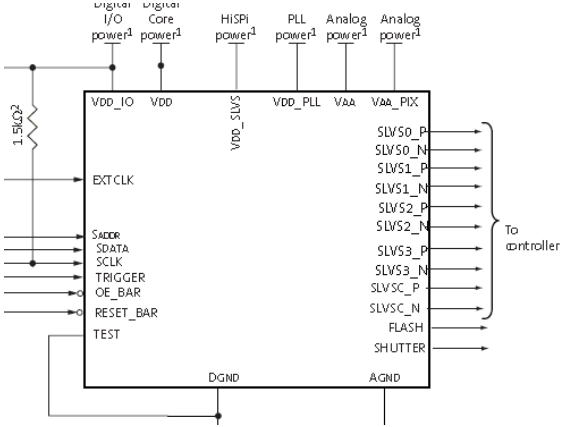
Evolution of Image Sensor interfaces

Parallel CMOS interface



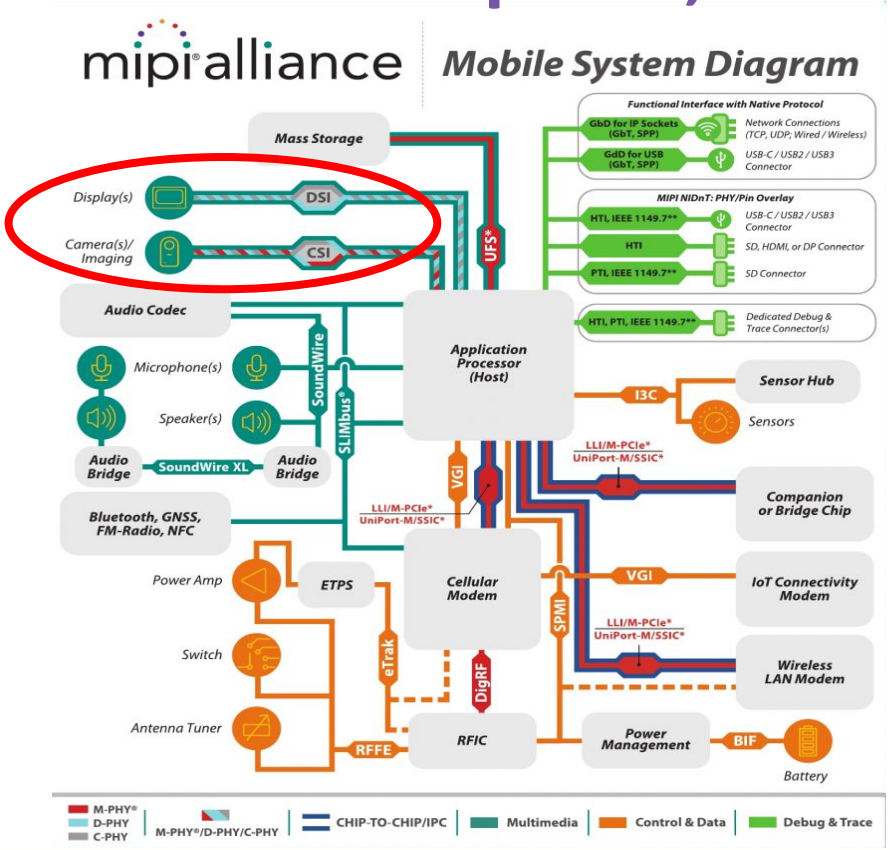
~ 2-3MP

subLVDS / HiSPi interface / etc.



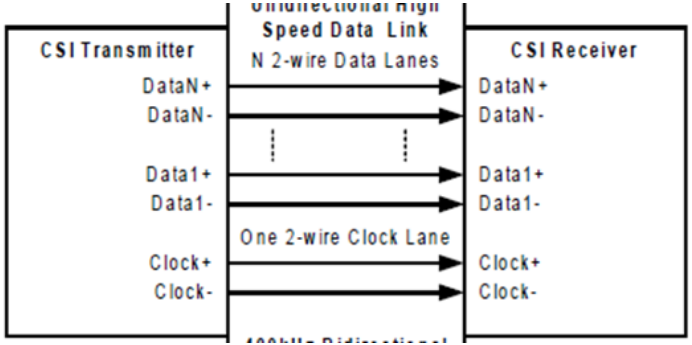
In 90's & 2000s parallel interface was the norm
In the next decade various proprietary interfaces were introduced

As Mobile Platforms Explode, So does MIPI CSI-2SM



Because of mobile popularity everyone drifted to CSI-2SM

- Just like a decade ago when PC components were used broadly, as mobile adoption exploded, so did the acceptance of MIPI CSI-2



Imaging Applications using FPGAs

Defense & Aviation

HMI & Displays

Time Lapse Camera

Automotive

Surveillance & IP Cameras

Machine Vision & Medical

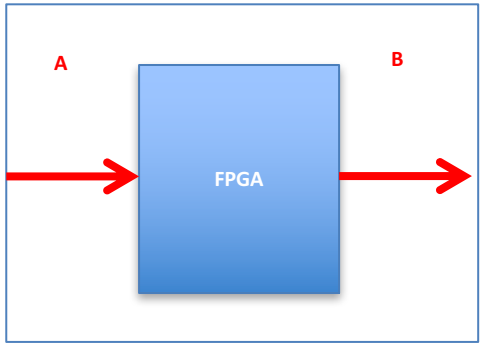
Infrared Camera

Why Use FPGAs?

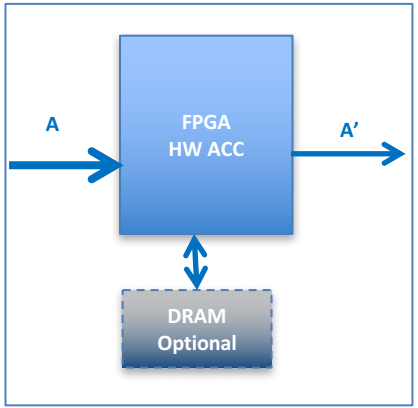
- Need multiple MIPI CSI-2 or other camera inputs and an AP/ISP does not have those
- An FPGA can implement a complete ISP
  - The embedded memory, math blocks and logic are a good match
- FPGA may perform some processing allowing for a lower cost AP/ISP
- Require multiple ISP engines
- Newer capabilities that are not available with an AP/ISP

FPGAs in imaging/video applications

Bridging



Acceleration

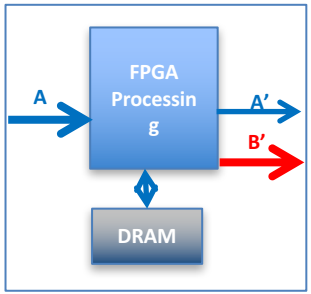


Bridging is the simplest designs

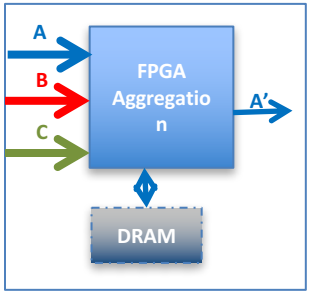
Acceleration requires more performance & capabilities

Processing & Aggregating with FPGAs

Processing



Aggregation

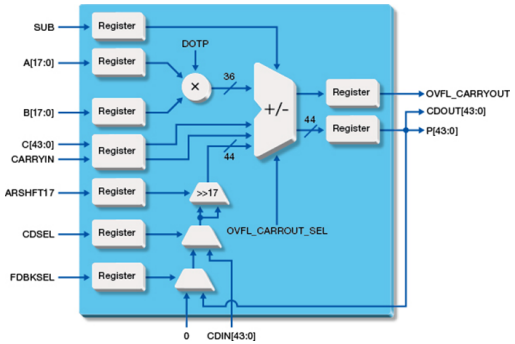


Processing could be in an embedded processor or with FPGA fabric, memory and Math blocks (DSP blocks)

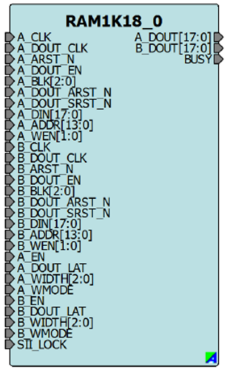
Aggregation leverages the large I/O capability of FPGAs and the fabric

Key Blocks used in FPGAs for imaging

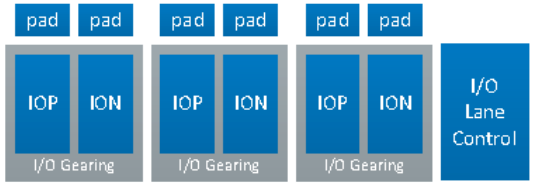
Math Blocks/DSP



Memory Blocks



I/O Gearing

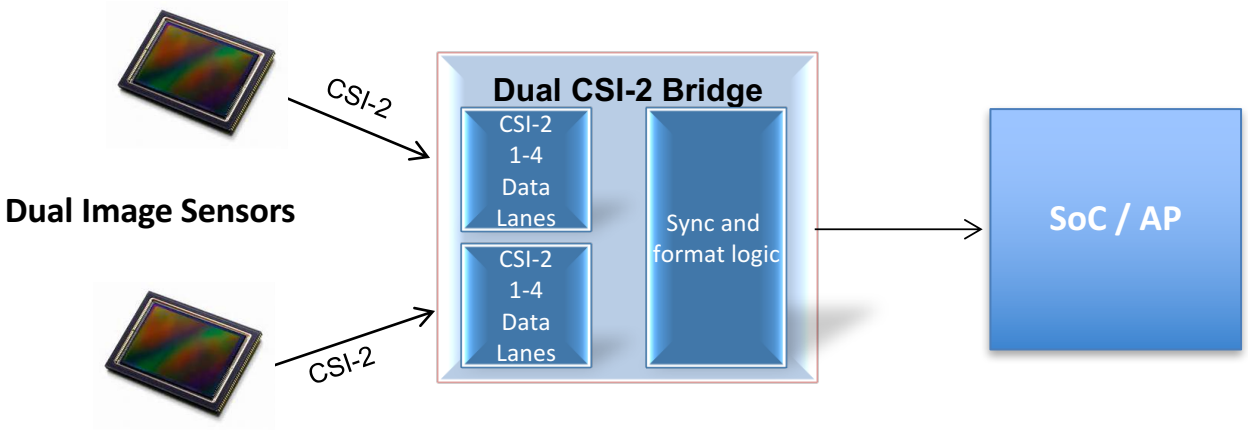


Processor/Micro

Multi-Camera Applications with MIPI CSI-2

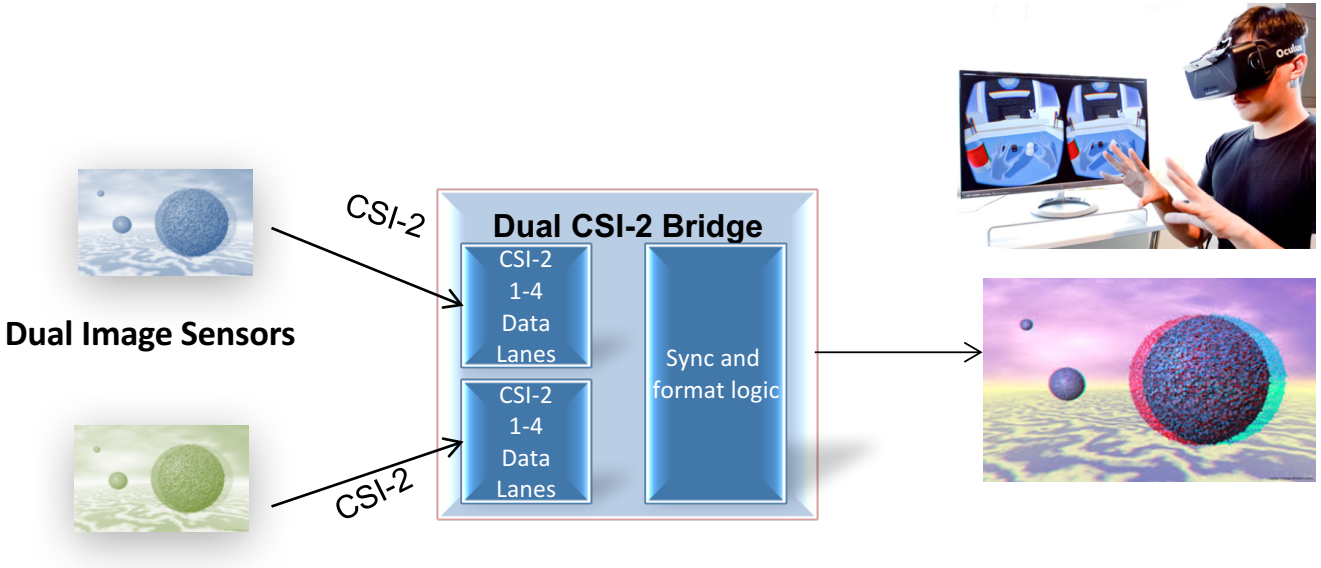
- 3D camera / Virtual Reality
- Dual Surveillance
- Multiple Image Sensor HDR
- 180 Degree Surveillance
- 360 Degree Panorama
- Surround View Automotive
- Depth Detection Applications
- Drone Usage

3D Camera Example



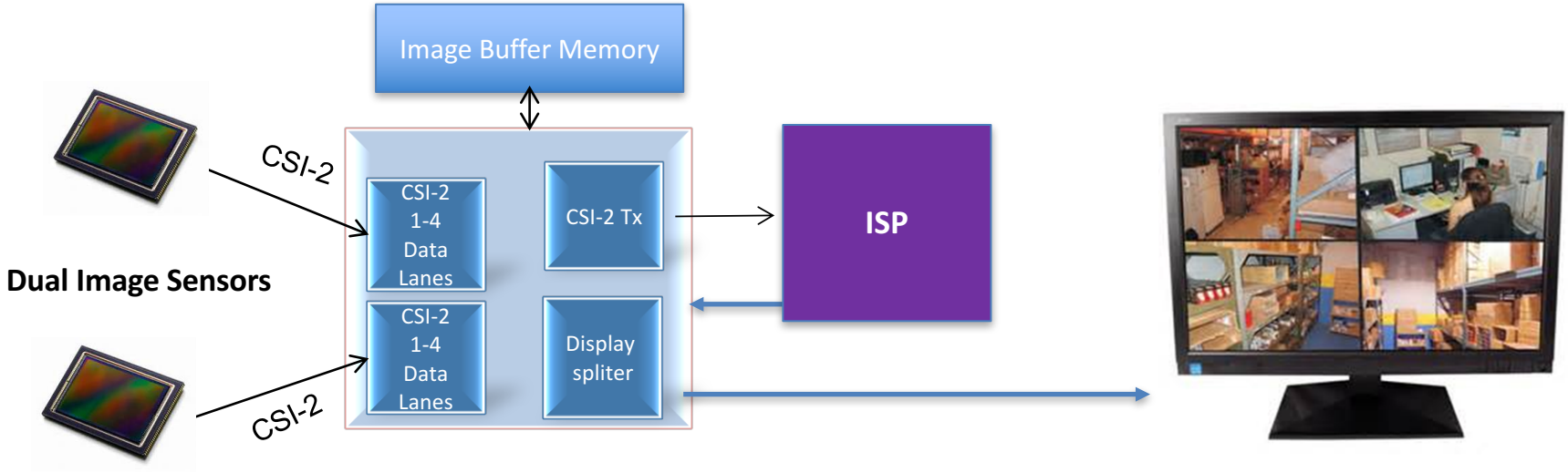
Although ISP devices often have multiple camera inputs they often benefit from an FPGA, which helps in synchronizing the image sensors & arranging them

3D Camera FPGA Implementation



The FPGA can arrange the image in a side by side or a top bottom configuration
This makes it easier for the ISP or AP to process the image

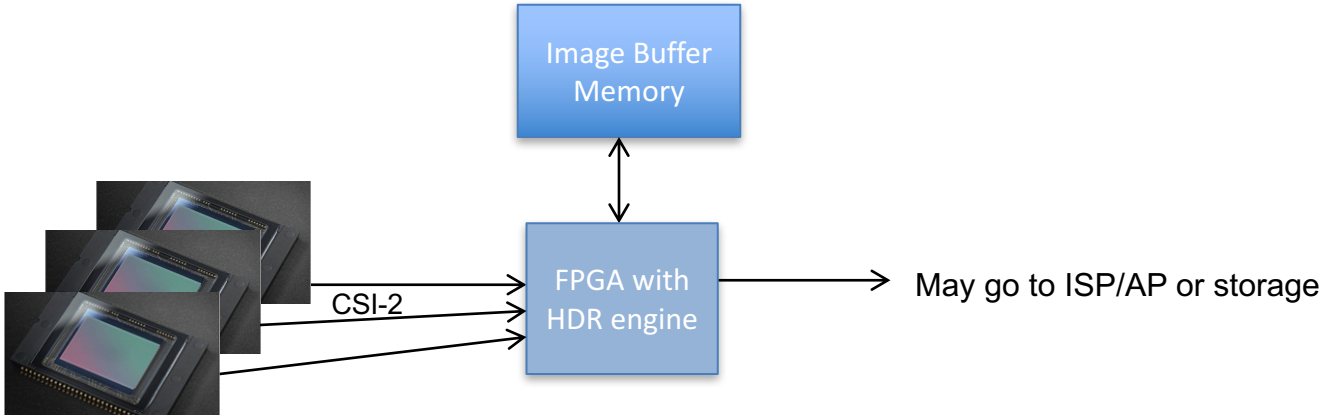
Dual Surveillance camera



Although ISP devices often have multiple camera inputs they often benefit from an FPGA which can arrange the image

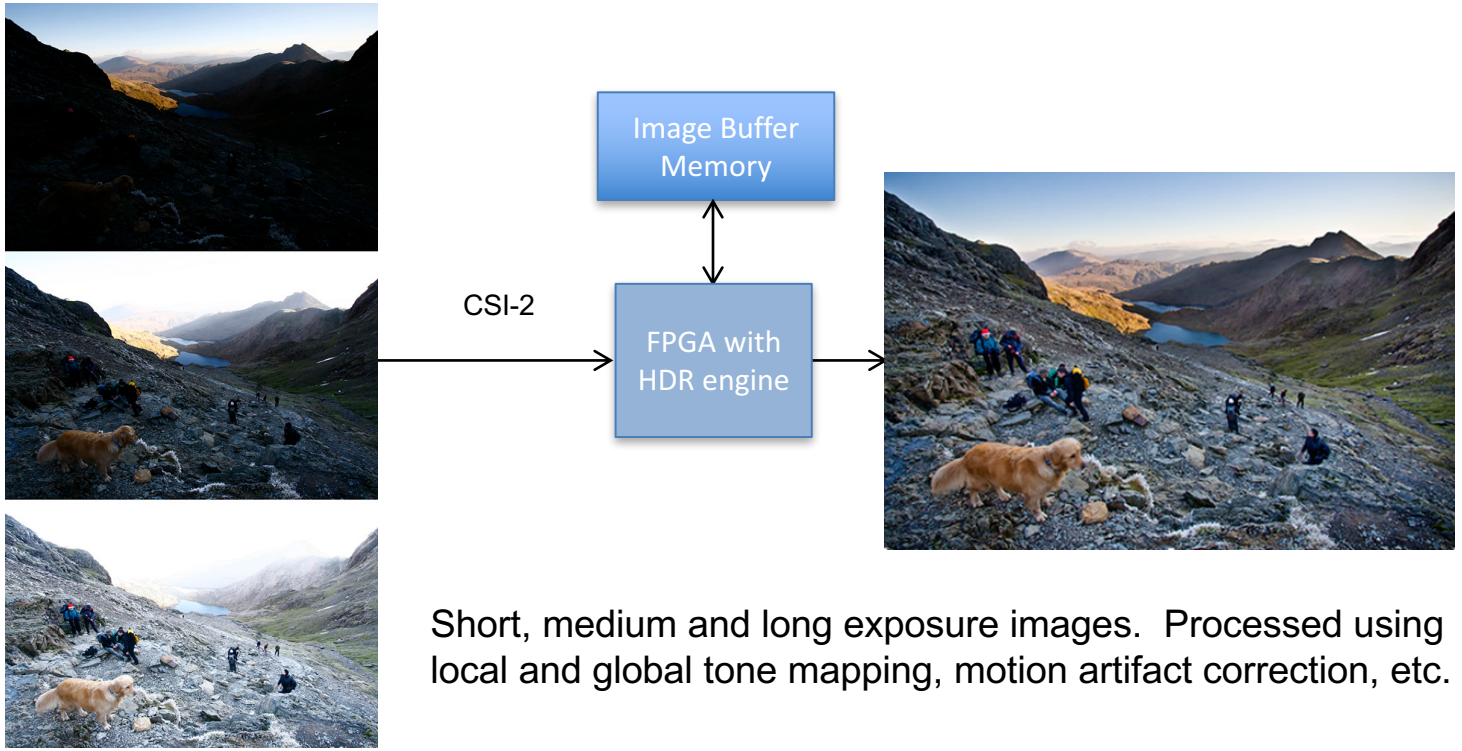
- Both images are recovered in the FPGA
- The FPGA combines the two images into one for the ISP – often a top bottom configuration
- This allows as ISP to process the two images as one, but the output can be split into two images

Image Sensor HDR processing



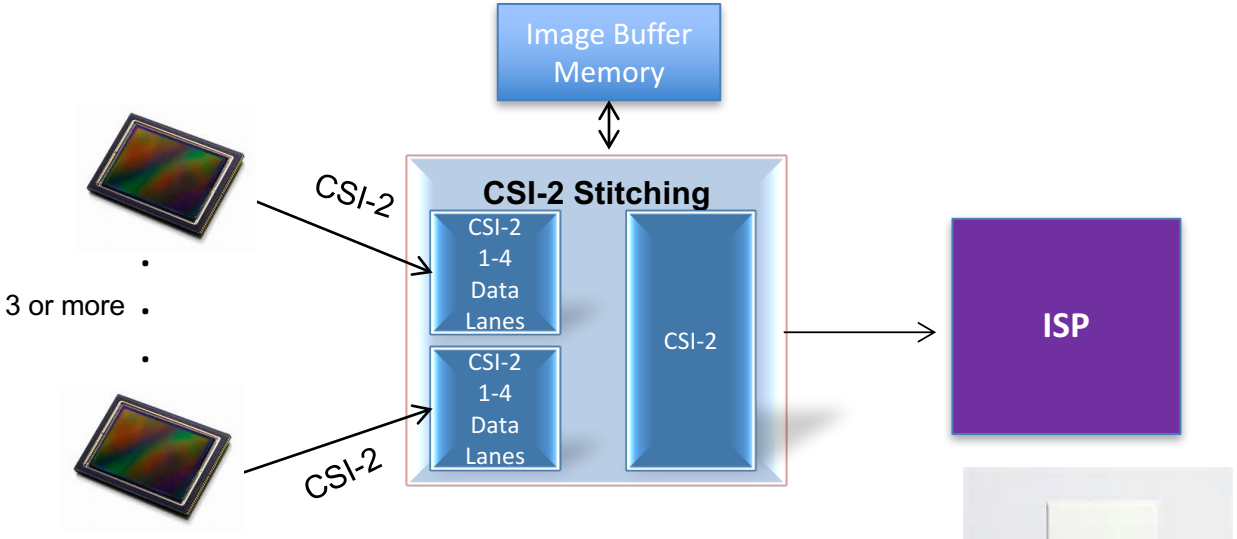
Each image sensor captures frames at exactly the same time. A short, medium and long exposure is used for each.

Image Sensor HDR processing



Short, medium and long exposure images. Processed using local and global tone mapping, motion artifact correction, etc.

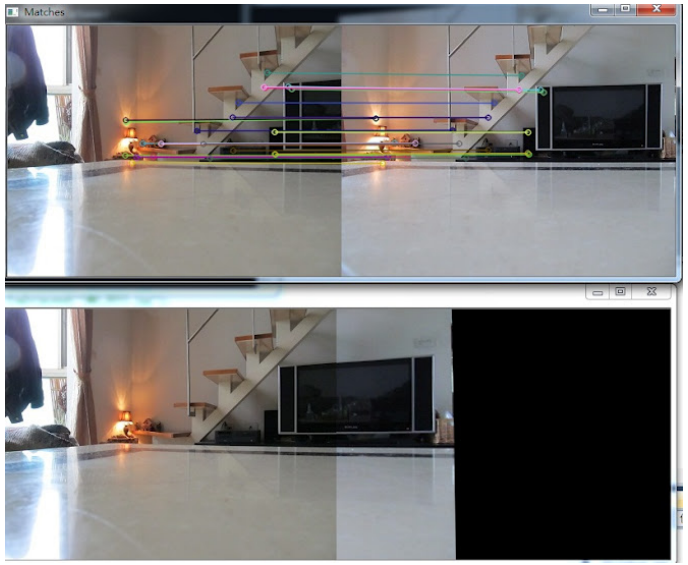
180 degree Surveillance camera



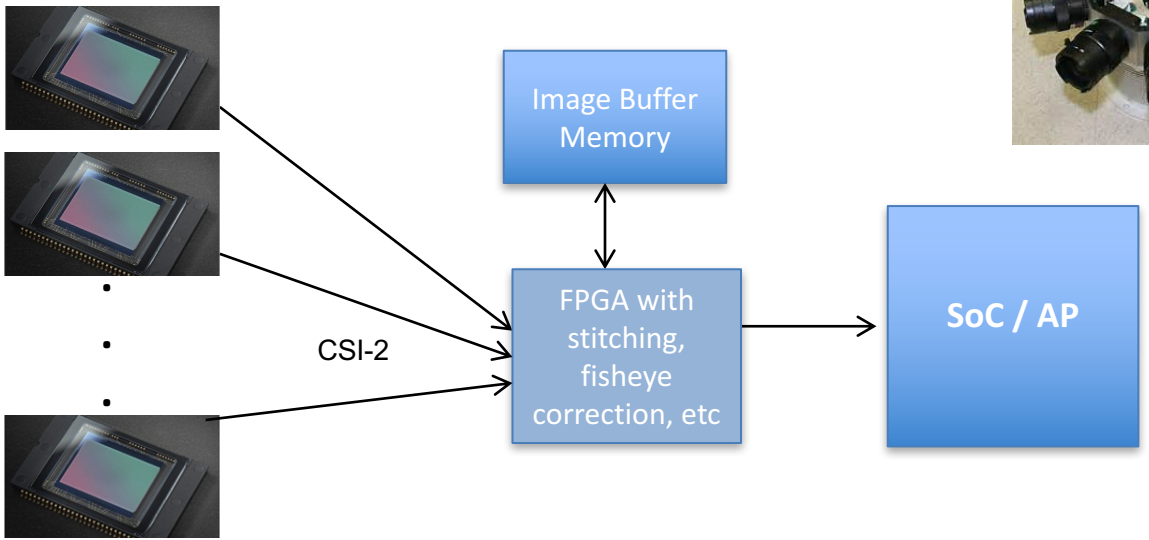
The image stitching function is more easily done in an FPGA
In this design the entire ISP could also be in the FPGA

180 Degree Surveillance FPGA Function

- Multiple images are recovered in the FPGA
- The frames are stored likely in external memory
- The FPGA performs an analysis to determine where to merge the image
- The images are stitched together
- Also likely a smoothing technique is used
- The image output is then processed in the FPGA or formatted and passed onto the ISP or AP



360 Degree Cameras

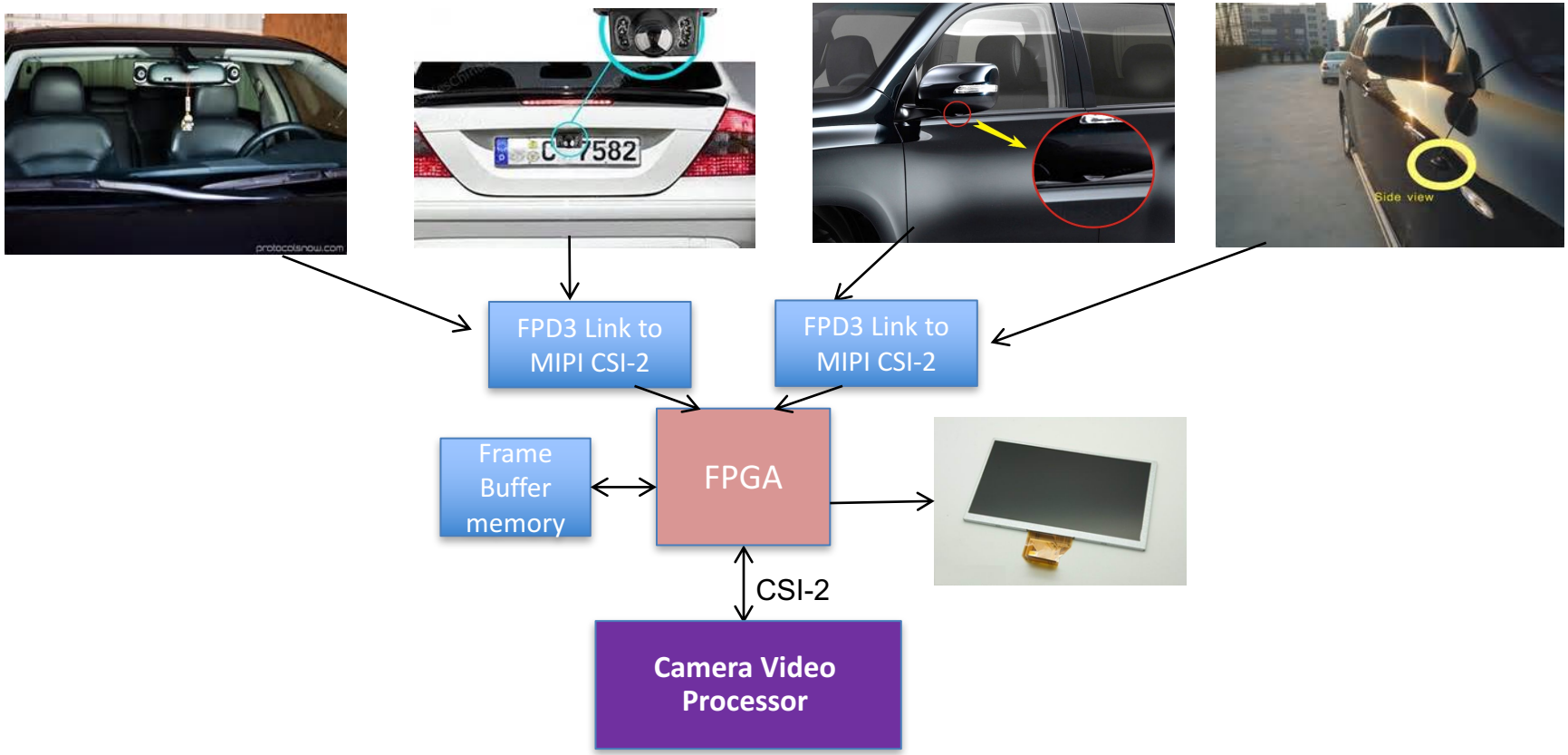


Each image sensor frames are captured and combined.
Image processing could be in the FPGA or AP/ISP

360 Degree Cameras

- The FPGA performs an analysis to determine where to merge the images
- The images are stitched together
- Depending on the output format, fisheye correction may be implemented
- The image output is then processed in the FPGA or formatted and passed onto the ISP or AP

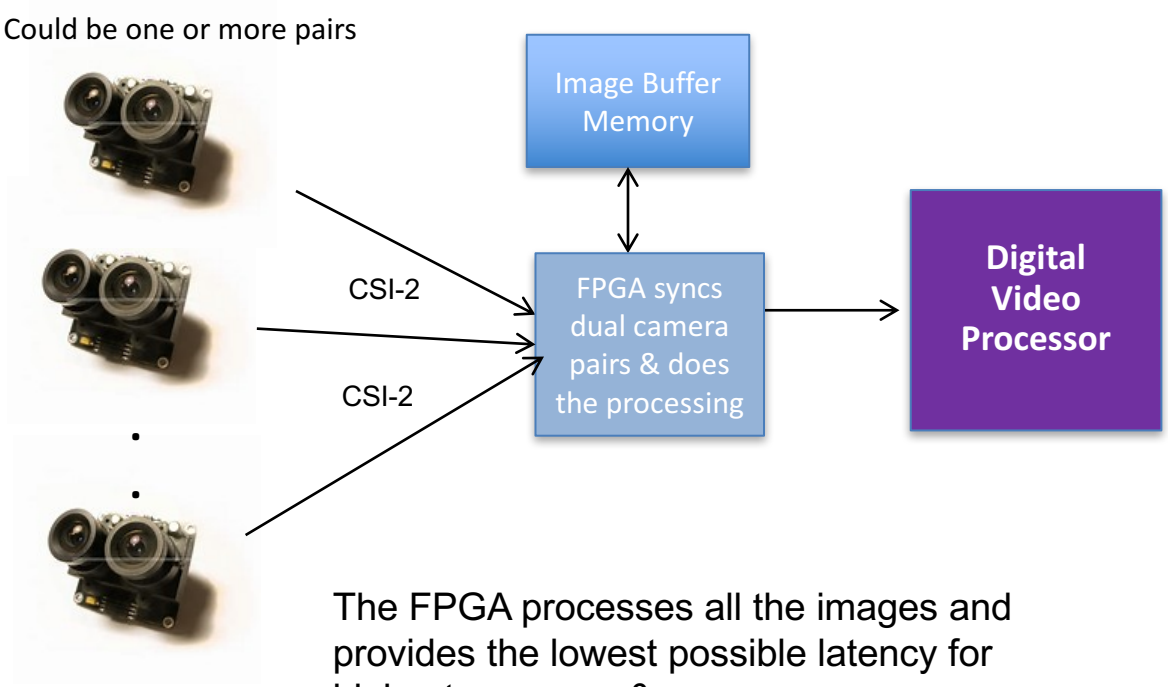
Surround View Automotive



Surround View Application

- The FPGA implements the stitching of the images
- It formats the image for the ISP/AP
- or FPGA processes the image and drives the display
- FPGA could add overlay such as directional lines

Multi camera for depth detection

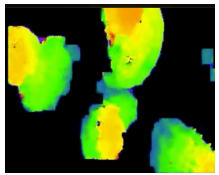


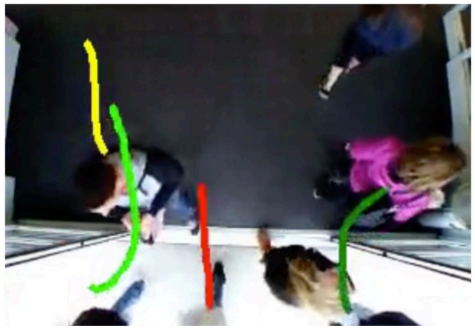
The FPGA processes all the images and provides the lowest possible latency for highest accuracy & response.

Multi cameras for Depth-Based Analytics

Dual Image Sensors

Top-Down Depth Image

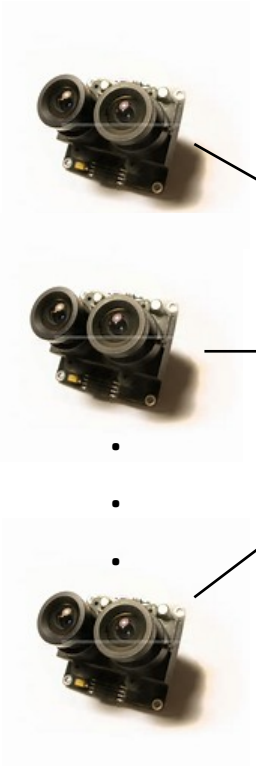


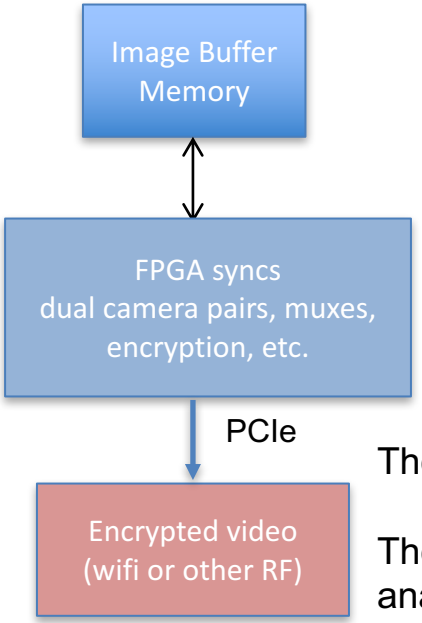


FlowMetrics™ by PercepTonic

The FPGA or AP computes 3D point cloud from a top-down stereo pair.
Depth-based analytics can distinguish adults, kids, people from shopping carts for accurate people counting.
The FPGA synchronizes each camera pair and processes what each camera pair sees
Parallel processing of the FPGA gives quickest response & accuracy

Multi camera Drone Application





These dual cameras allow a drone to “see”

The FPGA can merge, mux, pre-process, and run analytics pre-processing before the AP gets involved for 3D point cloud.

Summary

- Rapid adoption of MIPI CSI-2 in applications such as surveillance, automotive, drones, robotics and machine vision
- FPGAs provide a big advantage in multiple camera design due to parallel processing, abundant I/Os and easy interfacing with ISP/AP/Processors
- Most multi-camera applications require a mid-range FPGA which can optimize costs and performance (low-power, reliability and security)

mipi®
DEVCON

THANK YOU

2017
MIPI ALLIANCE
DEVELOPERS
CONFERENCE

BANGALORE, INDIA

MIPI.ORG/DEVCON