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Meeting the Needs of Next-Generation Displays with a High-Performance MIPI DSI-2™ Subsystem Solution
Bandwidth Challenge for Video Connectivity

![Graph showing bandwidth requirements over time for different categories like AR/VR, Auto, Tablets, and Mobiles. The x-axis represents years from 2008 to 2026, and the y-axis represents Gbps. The graph indicates a steady increase in bandwidth requirements.]
Bandwidth Challenge for Video Connectivity

![Graph showing the increase in bandwidth requirements from 2008 to 2026 for different device categories: AR/VR, Auto, Tablets, and Mobiles. The graph indicates a significant increase in bandwidth demand, with the PHY layer showing a more modest increase compared to the DISPLAY layer.]
Some Applications Require Even More Bandwidth

Mobile Displays
- Need to support gaming
- Need to be “AR/VR ready”
- Foldable displays
- Require higher display resolutions and frame rates

AR/VR Displays
- Need to drive two displays
- Require higher pixel density (ppi), higher pixel resolutions (bpc) and frame rates

Automotive Displays
- More displays
- Require higher resolutions
- Multiple input sensors
Gap between transport bandwidth and display requirements can be solved with compression.
Dual link configuration shown; single link also supported. Dotted line shows second link.
Hardent VESA DSC Compression IP
About Hardent

- First IP provider to bring VESA DSC IP cores to market in 2014

- VESA DSC IP cores are silicon proven
  - Over 100 design wins across a wide range of industries

- Active contributor to industry standards organizations
  - VESA member since 2013
  - MIPI Alliance member since 2015
VESA DSC Algorithm Overview

• Visually lossless video compression standard
• Compression as low as 8bpp without any perceptible differences
• Extremely low latency
• Video quality **excellent** with all types of content
  • Natural and test images, text, and graphics
• Requires a single line of pixel storage + rate buffer
• Intra-frame Variable Bit Rate Encoder
• Constant Bit Rate (CBR) transmission
• Based on Delta Pulse Code Modulation (DPCM)
• Mid Point (MPP), Block Predictor (BP)
• Modified Median Adaptive Predictor (MMAP)
• Indexed Color History (ICH)

Source diagram: VESA DSC white paper
Applications Using VESA DSC

- Mobiles
- Tablets
- Test Equipment
- GPUs
- AR/VR head-mounted displays
- In-car video systems
- Video transport
- 8K TVs
- DTV STBs
- High-res. monitors
Hardent DSC 1.2a IP: Key Features

• Backward compatible with DSC v1.1
• Supports all DSC mandatory and optional encoding mechanisms
  • Modified Median Adaptive Predictor (MMAP), Block Predictor (BP), Mid Point (MPP)
    and Indexed Color History (ICH)
• Transport stream agnostic
• Scalable number of parallel hard slice instances (1, 2, 4, and 8)
• RGB 4:4:4, YCbCr 4:2:0, and YCbCr 4:2:2 native coding
• 8, 10, 12, 14 and 16-bit video components
• 3 pixels / clock internal processing decoder architecture
• 1 pixel / clock internal processing encoder architecture
• Optional DSC features can be disabled to improve area (decoder only)
• Verified against VESA DSC C-model using comprehensive test image library
Hardent DSC 1.2a IP: Key Features

**Hardent DSC v1.2a Decoder IP**
- Multiple parallel decoder instances
- Single or multiple inputs
- Rasterized output
- Error resilience
- Low power & high performance

**Hardent DSC v1.2a Encoder IP**
- Multiple parallel encoder instances
- Single input with de-rasterization or multiple inputs
- Single multiplexed output or multiple outputs
- Synchronous or asynchronous dataflow
- MIPI DSI command mode supported
- Low power & high performance
DSC Helps Save Power, Area, and Cost

Application Processor

MIPI DSI Tx

DSC Encoder

MIPI DSI Tx

Display Driver IC

MIPI DSI Rx

DSC Decoder

MIPI DSI Rx

Remove SDRAMs

Frame Buffer

SDRAM

SDRAM

SDRAM
Rambus is a Leading Provider Of MIPI Controller Cores

- Rambus has been supplying MIPI Controller cores since 2010
  - Optimized 2nd generation CSI-2 and DSI-2 Controllers available
  - Fast deployment of new standards
  - Full featured
  - Full support for C-PHY/D-PHY
  - Full support for DSC
- MIPI Controller Cores widely used in ASIC and FPGA
  - 100+ ASIC design wins
  - 130+ FPGA design wins
- Delivered fully integrated and verified with ASIC PHY
  - Comprehensive PHY integration and validation process
DSI-2 Controller Core Key Features

- Fully DSI-2 Specification compliant
- PHY Support
  - 1-4 D-PHY lanes
  - 1-4 C-PHY lanes
- 32 and 64-bit core width versions
  - Support for all data types
- Flexible packet interface
- Support for extended virtual channels
  - Optional DSI-2 Video Interface
- Support for Hardent DSC
- Delivered fully integrated with target MIPI PHY
- Minimal ASIC gate count
- Provided with expert technical support
- Provided with a DSI-2 Testbench
- Customization and integration services available
- Support for FPGA prototyping
  - Off the shelf or with PHY test IC
DSI-2 Video Interface

- DPI-2\textsuperscript{SM} standard was established prior to the MIPI DSI standard
  - Hsync/Vsync style interface
  - Single pixel per clock
  - Limited data types (RGB 16/18/24 bit)
- DSI-2 Video Interface is a superset of DPI-2 Interface
  - Multiple pixel per clock support
  - All DSI-2 data types (RGB, YUV, etc.)
  - Minimized FIFO size relative to DPI-2 Interface
  - Enhanced sync retiming support
  - Enables Hardent DSC integration
About Mixel

- Leading provider of mixed-signal IP since 1998 with emphasis on PHY including:
  - MIPI PHY: D-PHY, C-PHY, M-PHY®
  - LVDS SerDes
  - Multi-standard SerDes: C-PHY/D-PHY, LVDS/D-PHY
- Industry leader in MIPI® interfaces and contributing member of the MIPI Alliance since 2006
- Complete integrated solution includes PHY, controller, and platform
- First IP provider to demonstrate silicon-proven D-PHY, C-PHY, and M-PHY
- Widest coverage of process nodes and foundries: silicon-proven in 11 different nodes and 8 different foundries
MIPI PHY Applications

- Requiring high bandwidth, low power and minimal area:
  - Mobile
  - Automotive
  - IoT/Sensor
  - VR/AR/MR
  - Other consumer electronics

(MIPI alliance, 2020)
Mixel MIPI C-PHY/D-PHY Combo

- Combo PHY can be configured as either a C-PHY or D-PHY
- Configurable for transmit (TX) and receive (RX), plus additional optimized configurations for TX and RX provide smaller area and higher performance
- Supports Camera Serial Interface (MIPI CSI-2) and Display Serial Interface (DSI, DSI-2)
- MIPI D-PHY mode supports MIPI D-PHY v2.5 Specification
- Up to 4.5 Gbps data rate per lane with De-skew calibration
- Up to 4 lanes, 18 Gbps aggregate bandwidth
- MIPI C-PHY mode supports MIPI C-PHY v2.0
- 80 Msps to 4.5 Gsps symbol rate per lane in high-speed mode
- Up to 3 trios, 13.5 Gsps/30.78 Gbps aggregate bandwidth
Multiple Generations of Mixel MIPI IP

Mixel MIPI D-PHY

D-PHY @ 2.5 Gbps

D-PHY @ 4.5 Gbps

Mixel MIPI C-PHY

C-PHY @ 2.5 Gbps

C-PHY @ 4.5 Gbps
Use Cases: Mobile, AR/VR & Automotive
Mobile Market Trends

- Mobile devices need to be XR-ready
- Movement from LCD to OLED displays with sub-pixel rendering
  - Ultra-high resolutions and pixel density (up to 1500 ppi)
  - High dynamic range (HDR)
  - Higher frame rate
  - Optical compensation
  - Foldable, rollable displays
  - Lower power consumption
  - Non-uniformity compensation
- DDIC frame buffer going from 10 to 100 Mbits

<table>
<thead>
<tr>
<th></th>
<th>2010</th>
<th>2020</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Display Resolution</strong></td>
<td>1280 x 720 HD</td>
<td>3840 x 2160 4K</td>
</tr>
<tr>
<td><strong>Frame Rate</strong></td>
<td>60 fps</td>
<td>120 fps</td>
</tr>
<tr>
<td><strong>Pixel Depth</strong></td>
<td>24 bits</td>
<td>30 bits</td>
</tr>
<tr>
<td><strong>Interface</strong></td>
<td>0.5 Gbps / lane</td>
<td>2.0 Gbps / lane With DSC</td>
</tr>
<tr>
<td><strong>Display Bandwidth</strong></td>
<td>1.3 Gbps</td>
<td>29.9 Gbps</td>
</tr>
</tbody>
</table>

23x
Use Case: Mobile and Tablet Applications

- Benefits
  - Reduce bandwidth
  - Save power
  - Lower EMI
  - Lower cost
  - Smaller footprint
  - Less pins
  - Lower switching frequencies
# D-PHY Speed/Display Resolution

## D-PHY v1.1 1.5 Gbps / lane

<table>
<thead>
<tr>
<th>Resolution</th>
<th>FHD (1080x1920)</th>
<th>WQHD (1440x2560)</th>
<th>WQXGA (1600x2560)</th>
<th>UHD (2160x3840)</th>
<th>WQUXGA (2400x3840)</th>
<th>5K (2880x5120)</th>
<th>8K (4320x8192)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>3.58Gbps</td>
<td>6.37Gbps</td>
<td>7.08Gbps</td>
<td>14.33Gbps</td>
<td>15.93Gbps</td>
<td>25.49Gbps</td>
<td>61.16Gbps</td>
</tr>
<tr>
<td>No compression</td>
<td>3 lanes</td>
<td>6 or 8 lanes</td>
<td>6 or 8 lanes</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>2x compression</td>
<td>2 lanes</td>
<td>3 lanes</td>
<td>3 lanes</td>
<td>8 or 6 lanes</td>
<td>8 or 6 lanes</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>3x compression</td>
<td>1 lane</td>
<td>2 lanes</td>
<td>2 lanes</td>
<td>4 lanes</td>
<td>4 lanes</td>
<td>8 lanes</td>
<td>N/A</td>
</tr>
</tbody>
</table>

## D-PHY v1.2 2.5 Gbps / lane

<table>
<thead>
<tr>
<th>Resolution</th>
<th>FHD (1080x1920)</th>
<th>WQHD (1440x2560)</th>
<th>WQXGA (1600x2560)</th>
<th>UHD (2160x3840)</th>
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<td>3 lanes</td>
<td>4 lanes</td>
<td>N/A</td>
</tr>
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AR/VR Market

• Challenges
  • Requires 2 displays at higher resolution, higher PPI, higher refresh rates

• Tethered HMD
  • Cables are running out of bandwidth

• Wireless HMD
  • Bandwidth, power management, and miniaturization are huge obstacles
Use Case: AR Head-Mounted Display (HMD)

HMD AR System With Frame Buffer

Applications
- Images captured by 3D camera
- Video and graphics processed by AR processor and GPU
- L/R video streams sent to micro-displays (DSI-2 Link)
- Video stored inside micro-display driver IC (Frame Buffer)

Benefits
- Lower bandwidth
- Smaller RAM buffer
- Power and $ savings
- Low latency
Automotive Market

• The number of displays and cameras in cars is increasing rapidly
  • ADAS, ACAS, infotainment, control panels, rear seat displays, head-up displays, side and rearview mirrors, …
  • 1-3 displays → 10-12 displays
  • 1 camera → 5-10 cameras
  • 2-5 sensors → 10-20 sensors

<table>
<thead>
<tr>
<th>Display Type</th>
<th>Spatial Resolution</th>
<th>DPI (pix / inch)</th>
<th>Bandwidth Req. @ 60 Hz refresh</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mid-range car</td>
<td>HD</td>
<td>1280 x 720</td>
<td>100</td>
</tr>
<tr>
<td>High-end car</td>
<td>FHD</td>
<td>1920 x 1080</td>
<td>200</td>
</tr>
<tr>
<td>Next-gen. car</td>
<td>UHD</td>
<td>3860 x 2160</td>
<td>400</td>
</tr>
</tbody>
</table>
Automotive Video Applications

Benefits
- Smaller bandwidth required for multiple feeds
- Low latency
- Save on expensive cabling
- Lower EMI
Integrated IP Subsystem Solution
Dual link configuration shown; single link also supported. Dotted line shows second link.
# DSI-2 DSC IP Subsystem Deliverables

## DSI-2 Controller Core Deliverables
- DSI-2 Controller Core – Source Code
  - Fully configured for application
  - Fully integrated and verified with D/C-PHY
  - User Guide, integration guide, timing constraints
  - Optional FPGA prototyping
- Testbench – Source Code
  - DSI-2 Peripheral or Host Testbench with DSI-2 Host or DSI-2 Peripheral BFM and C-PHY/D-PHY Behavioral Model
  - Expert Technical Support
    - One year of expert technical support
    - Optional services available (IP customization, logic development, etc.)

## DSC 1.2a IP Core Deliverables
- Encrypted synthesizable RTL code
- 100% verification coverage using a comprehensive UVM verification environment
- Functional and structural verification coverage reports
- IP testbench for post-synthesis verification
- Comprehensive integration guide
- Technical support

## C-PHY / D-PHY IP Core Deliverables
- Data Sheet/Specifications
- Integration guidelines
- GDS II data base
- LEF file
- LVS netlist
- Timing model
- Verilog model
- IBIS model
- RTL
- Test Benches
- First-class customer support through production
IP Integration Benefits and Conclusion

• Lower project risk with a fully integrated and verified IP solution
• Maximized functionality and availability of all MIPI DSI-2 operating modes
• Optimized for ASIC design performance (PPA)
• Accelerate ASIC and SoC time to market
• Immediate availability
Demo

View a demo of the IP subsystem later today

08:05 to 08:15 PDT
More Information

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