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I3C® Signal Integrity Challenges on DDR5 Based Server Platform Solutions
Agenda

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Introduction
Introduction

- The MIPI I3C Improved Inter-Integrated Circuit interface is first introduced in a server application for the DDR5 DIMM Serial Presence Detect ( SPD) function.

- Its implementation exceeds by far the bus capacitance/loading specification, which was defined for low capacitance Mobile/IoT applications.

- This presentation covers the interoperability challenges of the dynamic push-pull and open-drain operating modes on I3C BASIC server applications.
  - Covering an in-depth analysis of the implications of long PCB traces, multiple DIMM routing branches, several loads, to the electrical and timing parameters.
Introduction cont'd

• I3C Communication Bus specification was released by MIPI Alliance in 2016, as an improved communication protocol compared to its predecessor I2C, but the implementation of I3C, in a Data Center (Server) application was materialized until 2020.

• The main enhancements in I3C adopted by the DDR SPD function are:
  – Higher bit rate: up to 12.5MHz, compared to 100KHz-1MHz I2C SPD in prior DDR generations (125x to 12.5x higher bit rate).
  – Better IO electrical interface: Push-pull driver vs Open Drain only.
  – In-band interrupts (IBI) support – Not supported in DDR5 now, but looking for support in the future (or in other Server use cases).
  – In band Common Command Codes (CCCs) – Direct or Broadcast.
  – Reduced interface power (1.0V IOs).
Introduction cont'd

- The DDR5 SPD interface transitioned from I2C to MIPI I3C based on the following requirements for the next generation DDR DIMM technology:
  - Lower IO operating Voltage (as low as 1V aligned to advanced process node)
    - DDR4 SPD IO voltage was 2.5V
  - Higher interface bit rate (400KHz to 8-12.5MHz in real applications) due to the increased number of devices per DIMM to be managed
    - DDR4 had two devices per DIMM vs five devices in DDR5
    - Considering 8 DIMMs per SPD segment, this is 16 vs 40 devices
  - Higher bit rate to reduce boot time (diminishing Memory Reference code execution time)
DDR5 SPD Server connectivity and bus characteristics
DDR4 vs DDR5 SPD DIMM Connectivity

- **DDR4 SPD**
  - I2C Platform Controller (CPU or BMC)
  - Level Shifter
  - I2C Platform Interface (2.5V)
  
- **DDR5 SPD**
  - I3C Platform Controller (CPU or BMC)
  - I3C Platform Interface (1.0V)
  
Provides isolation and transparent communication from the Host to the Local devices (5pf per device)
DDR4 vs DDR5 SPD DIMM Connectivity

- **DDR4 SPD**
  - I2C Platform Controller (1.0V or 3.3V) → Level Shifter → I2C Platform Interface (2.5V)

- **DDR5 SPD**
  - I3C Platform Controller (CPU or BMC) → I3C Platform Interface (1.0V) → Host Side Interface
  - SPID 3C Hub and Memory
  - Registering Clock Driver (RCD)
  - Power Management IC (PMIC)
  - Temperature Sensor #1 (TS1)
  - Temperature Sensor #2 (TS2)

Introduces a time delay (12ns round trip) between Host and Local Devices
DDR5 SPD Bus Characteristics
DDR5 SPD Platform Connectivity

- Host side Server PCB routing
  - Total length could exceed 50”
  - Server motherboards are BIG: up to 16”x 19”
    - BMC controller is located at the North side
    - DIMMs are located at the South side
    - CPU to DIMM SPD routing has lower priority than high speed IO routing (DDR5, PCIe G4/G5, etc.)
Routing length and capacitance

- **Host side Server PCB routing**
  - From Controller to DIMMs ($L_{11}+L_{12}+L_{2x}$): ~25”
  - DIMM routing ($L_{\text{DIMM}}$): 3.5”/DIMM, 28” 8x DIMMs
  - Total PCB trace length: ~53”

- **Host side Total Capacitance**
  - Each device apports 5pF
    - 1 CPU + 8 HUBs = 45pF
  - PCB routing is ~3pF/in
    - 53” * 3pF = ~159pF
  - Totaling:
    - Dev (45pF) + PCB (53pF) = ~204pF
I2C and MIPI I3C Retro-compatibility Challenges
I2C and MIPI I3C Retro-compatibility Challenges

• There are three operating modes supported by the I3C protocol:
  – I2C mode with Open-Drain(OD) buffer class.
  – I3C mode with Open-Drain buffer class.
  – I3C mode with Push-Pull(PP) buffer class.

• The OD class requires a pullup to set a stable “Logic-high”.
  • The pullup is set accordingly with the total capacitance on the bus.
  • High capacitance busses requires a “Strong pullup”
    – Strong pullup guarantees rise time specification to pass.

• The PP class requires a High-Keeper pullup.
  – A “Weak pullup” is required to the target device with low current can pull SDA signal low within a minimum low period.
    – Weak pull-up lessens the voltage levels disturbances

MIPI I3C Basic Spec requires Dynamic pull-up control to switch between “strong pull-up” and “weak pull-up” to optimize open-drain and push-pull timing requirements.
Non-Dynamic Pullup impact in a 204pF bus

 dbContext

Push-Pull

Open-Drain

The Highest the PU

- VIH never reached with pull-up higher than 800Ω
- Limit max operating frequency

- On-Board PU can guarantee an OD max operating frequency.
  - A parallel equivalent \( R_{PU,HK} \parallel R_{PU,OD} \) of 333.3Ω
    - Rise time=75.3ns
  - A pullup ≥ 550Ω negatively affects both rise time and operating frequency

A trade-off among pull-up value, rise time and \( V_{OL} \) is required to meet the highest operating frequency
Buffer $R_{ON}$ design implications
Buffer $R_{\text{ON}}$ value design implications

- The bigger the $R_{\text{ON}}$ the higher the $V_{\text{OL}}$ is:
  
  - Increasing trace length results in higher $V_{\text{OL}}$
    
    - With the longest trace length, $V_{\text{OL}} = 192\text{mV}$,
      
      - Assuming $V_{\text{IL}} = 0.3\text{V}$ then the transition margin is $108\text{mV}$
        
        » Low transition margin can cause idle states
  
- Setting the $R_{\text{ON}}$ at $40\Omega$ reduces the $V_{\text{OL}}$
  
  - With the longest trace length $V_{\text{OL}} = 146\text{mV}$,
    
    - If $V_{\text{IL}} = 0.3\text{V}$ then the transition margin is $154\text{mV}$

- Notice that at the longest trace length with $V_{\text{OL}} = 146\text{mV}$ the $I_{\text{OL}}$ is $3.66\text{mA}$

By limiting Ron into a max range of $40\Omega$ ensures a healthy $V_{\text{OL}}$ by setting a max $I_{\text{OL}}$ bigger than $3\text{mA}$
Critical time margin calculation
Critical time margin calculation

**TARGET driving to PRIMARY: Setup margin**

\[
T_{su_{\text{mar}}} = t_{\text{LOW}} - (T_{\text{fit,CLK PRIMARY-HUB}} + T_{pd_{\text{CLK HUB}}} + T_{\text{co,DATA HUB}} + T_{\text{fit,DATA HUB-TARGET}} + T_{pd_{\text{DATA HUB}}} + T_{\text{fit,DATA TARGET-HUB}} + T_{pd_{\text{DATA TARGET}}} + T_{\text{fit,DATA PRIMARY-HUB}} + T_{pd_{\text{DATA PRIMARY}}} + T_{su_{\text{margin}}} - T_{su_{\text{PRIMARY}}})
\]
Critical time margin calculation

<table>
<thead>
<tr>
<th>Frequency</th>
<th>10 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Duty cycle</td>
<td>35 %</td>
</tr>
<tr>
<td>tLOW</td>
<td>65 ns</td>
</tr>
<tr>
<td>tflt_CLK_PRIMARY-HUB_fall</td>
<td>19.1 ns</td>
</tr>
<tr>
<td>tpd_CLK_HUB</td>
<td>6 ns</td>
</tr>
<tr>
<td>tflt_CLK_HUB-TARGET_fall</td>
<td>4.7 ns</td>
</tr>
<tr>
<td>tco_DATA_TARGET</td>
<td>12 ns</td>
</tr>
<tr>
<td>tflt_DATA_TARGET-HUB_rise</td>
<td>1.972 ns</td>
</tr>
<tr>
<td>tpd_DATA_HUB</td>
<td>6 ns</td>
</tr>
<tr>
<td>tflt_DATA_HUB-PRIMARY_rise</td>
<td>9.8 ns</td>
</tr>
<tr>
<td>tsu_PRIMARY_max</td>
<td>3 ns</td>
</tr>
<tr>
<td>Setup Margin</td>
<td>2.253 ns</td>
</tr>
</tbody>
</table>

- The longer trace length the biggest flight time
- Inner device propagation delay plays a significant role in defining the operating frequency.
  - The highest the Tpd the bigger the time margin reduction.
- Increasing tLOW provides extra timing margin.
Frequency and AC/DC parameters impact

- Increasing duty cycle reduces $t_{LOW}$, thus reducing the Time Margin.
- When reducing the Duty Cycle the $t_{HIGH}$ and $t_{DIG\_HIGH}$ are affected.
  - Small Duty Cycle can produce a NOT PASS on $t_{HIGH}$/$t_{DIG\_HIGH}$.

A correct selection of Duty Cycle provides extra time margin to complete the setup transaction, granting higher operating frequency.

From MIPI I3C Spec $t_{HIGH\_min}$ 24ns, $t_{DIG\_HIGH\_min}$ 32ns
Non-monotonic signal behavior
Non-monotonic signal behavior

• Termination effect on transmission lines
  – Non-terminated circuit:
    • Signal bounces back and forth between the driver and the receiver.
  – Tx-terminated circuit:
    • Reduces drive strength
    • Increases propagation delay
    • Limits buffer capabilities
  – Rx-terminated circuit:
    • Reduces bouncing effect
    • Increases propagation delay
Slope reversal capability and timing improvement
Slope reversal capability and timing improvement

• With the non-deterministic loading of an unterminated bus, there can be reflections on the bus causing slope reversal on the Rx signal.
• By sampling at the first threshold is possible to filter Non-Monotonicity's; Schmidt triggered inputs
  – Non-terminated VS Rx-Terminated: Improves 2.3ns
  – Non-terminated VS Tx-Terminated: Improves 3.92ns

Slope reversal capability provides additional time margin that improves operating frequency and prevent false logic states.
Summary
Summary

- I3C Applications in Server systems (such as DDR5 SPD) are dealing with higher Bus capacitance than the max limit assumptions in MIPI spec (for 12.5MHz capable buses).
- Higher Bus capacitance applications can be mitigated by using good Buffer Drive strength, strong open-drain class pull-up, and HUB isolation circuits.
- A dynamic pullup operation allows to drive the interoperability challenges between the open-drain and push-pull operating modes; by enabling higher operating frequencies on both modes and limiting critical parameters to meet latest specification.
- Strong buffers tend to increase signal energy reflections, specially in complex topologies resulting with slope reversal conditions at Devices' Inputs.
- Schmitt trigger capable inputs are required in order to mitigate slope reversal conditions when dealing with high bus capacitance and strong buffers.
THANK YOU!