Subsystem and IP with MIPI bring Fast Time to Market for Mobile Application

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Outline

- Market Outlook – Mobility continues to be BIG!
- IP Solution – Raising demand for 3rd party IPs
- Subsystem with MIPI – Enables fast time-to-market
- Summary
Big Trends Creating Big Opportunities

Mobility continues to be BIG!

**Mobility**
- $141B in 2018
- 10.6% CAGR
- $77B in 2012

**Cloud**
- $21.0B in 2018
- 54.7% CAGR
- $1.5B in 2012

**Internet of Things**
- $8.9B in 2018
- 35.4% CAGR
- $1.4B in 2012

Source:
- Databeans, Cadence
- McKinsey, Cadence
- Gartner, IC Insights, Cadence
Mobile Device Powered by MIPI Interfaces

- More and more applications beyond mobile are adopting MIPI as interfaces.
- MIPI is working with other organizations to provide application solution, such as display (VESA), storage (JEDEC) and chip2chip communication (PCI-SIG/USB-IF)
- Enable customer’s applications using MIPI is getting more important
Mobile Beyond Smart Phones

- Wearable Technology
- Gaming platforms with WiFi
- Trackers with GPS and cellular data modems
- Video monitoring – Wi-Fi and/or cellular
- Payments terminals
- Mobile Routers
- Home Control
- Security Systems
- Automotive
IP Solution
Secret to Mobile Platform
Rising Demand for 3rd Party IP

Design of all IPs in-house is not practical

Demand for 3rd party IP is growing

Growing Number of IP Blocks in an SoC

Cadence®
World-class EDA → Leading IP portfolio

IPG

Tensilica®
Processor IP

Interface & memory IP

Verification IP
Cadence System Design Enablement
It takes an ecosystem

- Mechanical
- Software
- Standards
- PCB
- ODM
- Package
- IP
- EDA
- Foundry
- Semi
- Differentiated Product
- Form Factor, Cost
- Power, Performance, Area
- Mobility
- Cloud
- Internet of things
Cadence IP solutions enable the customization, integration, and verification of designs with confidence.
Cadence IP – A Path for Getting to Market Faster
A trusted partner enabling customer innovation

Design IP
- Fastest Growing segment share
- 1st to adv. nodes with DDR, PCIe
- Highest performance Analog IP

Tensilica® IP
- #1 in DSP IP segment share
- Shipping 2 Billion cores/year
- 200+ licensees world wide

Verification IP
- #1 in Verification IP Market segment share
- 100% adoption by top 30 semiconductor companies
- 500+ customers world wide
Cadence MIPI IP Solution

- MIPI Controller IP portfolio
  - CSI - Camera
  - DSI - Display
  - DigRF – Radio
  - SLIMbus - Audio
  - SoundWire – Audio
  - UniPro – Chip2Chip
  - UFS – Storage
  - M-PCIe – Chip2Chip
  - SSIC – Chip2Chip

- MIPI PHY IP
  - D-PHY
  - C-PHY
  - M-PHY
Complete IP Solution
Tailored to the Needs of Each Vertical Market
Subsystem with MIPI Enables Fast Time-to-Market
Typical Function Blocks in SoC Design

Challenge: Ever increasing effort on IP integration and system verification
Camera Processing System Trend

Imaging System:
- Low pixel size requires innovative noise reduction
- New Imaging Features:
  - Video image stabilization (iPhone6 & 6plus)
  - Fast AF: Galaxy S5, iPhone6
  - HDR
  - Dual Camera Support: HTC

Computer Vision:
- Addition of Computer/Machine Vision
- Face Detection: VGA to 720P
- Eye tracking

3D Capture:
- Which solutions:
  - Stereo? Array?
  - Structured light (Google Tango)
  - TOF

Flexible/programmable processor engine with low power consumption
Solving Complete Camera Pipeline

Type of Processing
- Lens Shading
- Defect Correction
- HDR
- Phase Detection AF
- Demosaic
- Color matrix
- 2D/3D Noise Reduction
- Image Stabilization
- HDR/WDR
- Super resolution
- Face Detection
- People Detection
- Object Detection
- Gesture Detection
- Motion Detection

Image processing

Vision processing

Tensilica IVP
### Cadence Camera/Display Subsystem

**Image & Vision processing**

- DMA
- I-RAM
- D-RAM

**Tensilica IVP_EP**

**2D/3D Noise Reduction**

- Image Stabilization
- HDR/WDR
- Super resolution

**Face Detection**

- People Detection
- Object Detection
- Gesture Detection
- Motion Detection

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**Integrated MIPI + IVP-EP Running Face Detection**

**Hardware Platform Features:**
- Input: 5MP Camera over MIPI CSI-2 interface
- Output: LCD display over MIPI DSI interface
- Integrated IVP-EP running at 60 MHz
- MIPI CSI-2 Rx and DSI Tx controllers
- 2-lane 1.5Gbps 28nm DPHY testchip daughter card
- DDR3 system memory

**Software Features:**
- Cadence Face detection software running on IVP-EP
- Detection done in every frame
- Camera detecting faces in realtime 15fps, VGA resolution
Audio Application Seeking Higher Performance and Less Power

- **Mobile – Smartphones, Tablets, Ultrabooks**
  - Audio and voice
  - Always On voice trigger, face trigger

- **Wearables – Smart watches, Glasses**
  - Always On voice trigger, face trigger
  - Audio and voice
  - Sensor Fusion
    - Indoor pedestrian location tracking - Pedestrian Dead Reckoning
    - Biometrics

- **Home Entertainment – DTV, STB, Gaming**
  - Audio codecs such as Dolby, DTS
  - Audio post processing
  - Interactive audio and voice codecs for real time gaming

- **Automotive – Digital Radio, Head Unit Infotainment**
  - HD Radio, DAB, DAB+, DRM, T-DMB, Sirius-XM
  - Audio codecs such as Dolby, DTS
  - Audio post processing, active noise cancellation
Cadence Audio Subsystem

Audio DSP Performance/Power Leadership
- Scalable family of audio DSPs address breadth of audio applications from mobile to home to auto.
- HiFi 3 – up to 1Ghz, (4x24 MACs or 2x32 MACs)
- HiFi 3 – 3.3 MHz MP3 decode, 16 MHz AACplus V2 decode
- HiFi Mini – As low as 16.6 μW for "always on" voice trigger in 28nm HPL

Comprehensive Audio SW and Ecosystem Offering
- 125+ codecs and audio enhancement packages
- All codecs are licensed, delivered and supported by Tensilica
- Optimized DSP math library
- 60+ Audio ecosystem partners

Flexibility to Achieve Optimal System Solution
- Easy integration with Soundwire/Slimbus Interface
- Configurability – Add/configure caches and local memory
- Extensibility – Custom instructions can be added with full compiler support
- High Level Programmability – World class ‘C’ compiler
Cadence UFS Turnkey Solution: UFS Host, UniPro, M-PHY

UFS: High Bandwidth & High IOPS
- Sequential Performance: Separate R/W channel + Scalability by/through Multiple Lanes (x1/x2/x4) and Gears (3.0Gbps, 6.0Gbps)
- Random Performance: Asynchronous Protocol (Command Queuing)

- Complete UFS Controller and PHY Solution
- UFS Software and Firmware
- Pre-integrated for fast Time-to-Market
- Performance Tuning Consultant
- UFS FPGA Board for early development

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Cadence Multi-Protocol PHY for Mobile Application
Flexible, Low Risk, Fast TTM, Attractive Cost

- **High Flexibility:** One design for multiple applications and use scenarios
- **Low Risk / Fast TTM:** One PHY to bring up, characterize and integrate
- **Attractive cost:** Shared components/logics, less IO for multiple interfaces
Mobile Enablement

• Requires a solid ecosystem – Mobile IP, tools flow and testing
• A full portfolio of Hard IP, Soft IP and VIP

Fast TTM with lowering risk

• IP that can be sourced from a single vendor
• Market/Application focused IP and Subsystem
• Silicon proven, integrated and verified IP

Cadence wants to be your reliable partner

• Providing a complete Mobile IP Portfolio
• MIPI IP that include Hard IP, Soft IP and VIP
• Providing access to HW boards for interoperability