A Developer’s Guide to MIPI I3C℠ Implementation

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Outline

- Introduction to MIPI I3C℠
- MIPI I3C℠ key feature descriptions
- Implementation guidelines
  - Legacy Device Support
  - HDR Modes
  - Varied Topologies
- Summarized good design practices
Welcome to MIPI I3C<sup>SM</sup>!

- An exciting new addition to the MIPI catalog
- Unifies key attributes of I<sup>2</sup>C and SPI, commonly used for Sensors
- Improves capabilities and performance
I3C<sup>SM</sup> for Ubiquitous Low Speed Interfacing

- Anywhere sensors are used, I3C<sup>SM</sup> belongs
- Aimed toward historical I<sup>2</sup>C, SPI and UART applications in...
What is MIPI I3C℠?

- Innovative new 2-Wire interface
- Key features address historical pain points
  - In-band Interrupt, Dynamic Addressing, Multi-Master, Standardized Commands, Time Control, Hot-Join, Error Detection and Recovery
  - Plus...

I²C Compatibility
Low Power
High Data Rates

Energy Consumption: mJ per mega bit for I3C data modes (100pF) vs I2C (100pF, 3.54KΩhm)

Data Rate: Mbps for I3C data modes (@12.5MHz) vs I2C (@400KHz)
Too Many I/Os!
Fragmented Interfaces!
MIPI I3C℠ Vision

- I²C Compatibility
- In-band Interrupt
- Common Command Codes
- Reduced Signal Count
- Reduced Interface Power
MIPI I3C℠ Features

- **I3C SDR – The Base Interface**
  - Up to 12.5 MHz I²C-like clocking with defined Open-Drain / Push-Pull
  - Supports multiple classes of Devices
    - I3C Main Master
      - SDR-only Main Master
    - I3C Secondary Master
      - SDR-Only Secondary Master
    - I3C Slave
      - SDR-Only Slave
    - I²C slave
MIPI I3C™ Features

- **SDR Dynamic Address Assignment**
  - Standardized procedure for dynamic assignment of 7-bit Addresses to all I3C Devices
    - I3C Slaves have two standardized characteristics registers and an internal 48-bit Provisional ID to aide the procedure
    - Legacy I²C Devices still use their static I²C Address

- **SDR In-band Interrupt**
  - Slave device can issue START Request when in “Bus Available” state
  - Master provides Interface Clock for Slave to drive it’s Master-assigned address onto the bus
  - Lowest assigned address wins arbitration in Open-Drain configuration
  - A data payload (i.e. Mandatory Data Byte) can immediately accompany the In-band Interrupt
MIPI I3C Features

- **Error Detection and Recovery Methodology**
  - For Master and Slave generated errors (9 Error Types identified, Parity, CRC5)

- **Common Command Codes**
  - Standardized command mode with extensible set of MIPI-defined codes that can be Broadcasted and/or Directed, Read and/or Write

<table>
<thead>
<tr>
<th>S or Sr</th>
<th>0x7E / W / ACK</th>
<th>Command Code</th>
<th>Data (Optional) (Broadcast CCC only)</th>
<th>Sr or P</th>
</tr>
</thead>
</table>

  - Standardized Command Codes
    - Event Enable/Disable
    - Activity States
    - Payload Mgmt
    - I3C Feature Mgmt (Dynamic Address Assignment, Mastership, HDR Modes, Timing Control)
    - Test Modes
    - Extensible Space (MIPI and Vendor)

* Example of Broadcast CCC Frame
Guidelines - Legacy I²C Device Support

- Fm and Fm+ Speeds Supported
- 50ns Spike Filter ($t_{SP}$) Needed for 12.5MHz I3C$^{SM}$ Clocking

$t_{SP}$: pulse width of spikes that must be suppressed by the input filter

- Clock Stretching is Not Allowed – I3C SCL is Push/Pull
- 20mA Open Drain Drivers ($I_{OL}$) are Not Used
- I²C Extended Addresses (10 bit) are Not Used
MIPI I3C℠ Features

- **I3C High Data Rate (HDR) Modes**
  - Optionally supported beyond the base SDR mode: 12.5MHz, SDA/SCL
    - HDR-DDR: Double Data Rate
    - HDR-TSL/TSP: Ternary Symbol
  - Offer bit rates over 33Mbps at a fraction of the per bit power of I²C Fast Mode
  - Simple Slave-side digital implementations
  - Coexistent with legacy I²C Devices
  - Leverage rising and falling edges
  - Individually entered using broadcasted MIPI-defined Common Command Codes
  - Universally exited and restarted via MIPI-defined toggling patterns
    - Allows non-HDR I3C Devices to “ignore” HDR transmissions

<table>
<thead>
<tr>
<th>I3C</th>
<th>Msg1</th>
<th>Msg2</th>
<th>I3C</th>
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<tbody>
<tr>
<td>START</td>
<td>Brdcst CCC</td>
<td>EnterHDRx</td>
<td>HDR Restart Pattern</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HDR Cmd</td>
<td>HDR Data</td>
</tr>
</tbody>
</table>

**Diagram:**
- **HDR Exit**
  - Setup (SDA/SCL) (If Needed)
  - Next Edge Confirms
- **HDR Restart**
  - SDA Restart
  - Setup (SDA/SCL) (If Needed)
  - Possible Restart
MIPI I3C™ Features

- **HDR-DDR: Double Data Rate**
  - Uses SCL as a clock, however Data and Commands change SDA on both SCL edges. By contrast, SDR Mode changes SDA only when SCL is Low.
  - HDR-DDR moves data by Words, which generally contains 2 preamble bits, 2 payload bytes and 2 parity bits. 4 Word Types are defined: Command Word, User Data, CRC Word, and Reserved Word.

- **Simple protocol:**

![Diagram showing SDA and SCL signals with P1, P0, D0.7, D0.6, D0.5, D0.4, D0.3, D0.2, D0.1, D0.0, D1.7, D1.6, D1.5, D1.4, D1.3, D1.2, D1.1, D1.0, P1, P0 notations.]

  - Preamble Bits: Define the subsequent Word Types.
  - Command, Data, or CRC: Based on Preamble (8bit MSB).
  - Parity Bits: P1: Odd Parity bit, P0: Even Parity bit.

Note: From Master to Slave: ACK = Acknowledge (SDA Low), NACK = Not Acknowledge (NACK), S = START Condition, Sr = START/Condition, P = STOP Condition, T = Transition Bit Alternative to ACK/NACK.
MIPI I3C\textsuperscript{SM} Features

- **HDR-TSL/TSP: Ternary Symbol Coding**
  - Ternary symbol coding for pure (TSP) and I\textsuperscript{2}C legacy-inclusive (TSL) systems
  - Given a two-wire interface with ‘simultaneous’ transitions and no traditional clock, there are 3 possible symbols available – 0, 1, 2
  - At least one line must transition each period
  - Ideally, there are 3 possible “next” transition
  - Transition indices are used to efficiently encode Binary into Ternary
  - Simple protocol:

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\[\text{SDA}\]

\[\text{SCL}\]

\[\text{HDR-TSL/TSP}\]

\[\text{I}\text{\textsuperscript{2}C and I3C SDR}\]

\[\text{data line stable; data valid}\]

\[\text{change of data allowed}\]
Guidelines - HDR Modes

• Enter HDR Commands Supported

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<td>HDR Restart</td>
<td>Pattern</td>
<td></td>
</tr>
<tr>
<td></td>
<td>HDR Exit Pattern</td>
<td></td>
<td>STOP</td>
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• HDR Exit Pattern detected by all I3C Devices

• Non-HDR Devices shall ignore I3C HDR bus traffic until the HDR Exit Pattern is detected
Guidelines - Varied Topologies

- Impacts on signal transition/transit times (maximum bus frequency)
  - SDA/SCL drive strength: “weaker” for lower power and interference vs “stronger” for faster over larger topologies/loads
  - Trace length and material: short vs long and pcb vs cable
  - SCL/SDA pad capacitance
  - Clock to Data Turnaround Time ($t_{SCO}$)
- Legacy I²C Devices impact maximum bus frequency (MHz)
  - Must run I3C at speeds/pulses beyond Spike Filter or slow Bus to that of slowest I²C Device
- Impacts on signal integrity/reliability
  - Device Location: close and far Devices can cause interference from reflections
Summarized Good Design Practices

• Thoroughly understand capability of coexistent Legacy I²C Devices
  – 50ns Spike Filter
  – Disabled Clock Stretch

• Understand bus topology and performance tradeoffs Mixed (I3C and Legacy I²C Devices) vs Pure Bus (I3C Devices Only)
  – Trace length and material
  – SDA/SCL pad capacitance
  – Clock to Data Turnaround Time ($t_{SCO}$)
  – Device location
Any Questions?