DigRF
BASEBAND / RF DIGITAL INTERFACE SPECIFICATION

Logical, Electrical and Timing Characteristics
EGPRS Version

Digital Interface Working Group
Rapporteur: Andrew Fogg, TTPCom

Version 1.12

REVISION HISTORY

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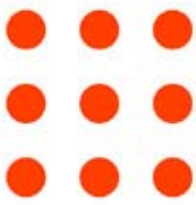
Sony Semiconductor and Devices Europe



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1 INTRODUCTION

1.1 Background

During the 1990s, silicon process considerations motivated a partitioning of the main functions of a GSM transceiver into three chips; baseband, mixed signal and RF. The analog interface between the mixed signal and RF devices evolved into a de facto standard of differential transmit and receive in baseband IQ format (sometimes multiplexed to save pins), together with analog AFC and PA power control. Improving silicon process technology and cost considerations are now motivating a new partitioning into just two chips, with some of the mixed-signal functions moving into the RF IC and others into the baseband. This new partitioning requires a digital interface, and it is clear that it would be helpful if this were to be a freely published standard. With this in mind a Working Group was formed to develop a suitable specification and place it in the public domain, in the hope that if it is supported by enough companies it will become the de facto standard for future chipsets. This document is that specification.

1.2 Purpose

The purpose of this document is to describe the logical, electrical and timing characteristics of the "DigRF" Digital BB/RF Interface with sufficient detail to allow physical implementation of the interface, and with sufficient rigour that implementations of the interface from different suppliers are "plug and play" compatible at the physical level. This version of the document addresses 2G/2.5G GSM (E-GPRS) implementations; later versions will extend the coverage to other standards and 3G.

Every effort has been made to retain flexibility where this does not compromise compatibility or cost, thus leaving many design choices within the baseband and RF IC implementations. The interface has been designed to support both direct conversion and near-zero-IF radios and location of the receive-path digital filter in either the baseband or the RF IC. On the Tx side, the RF IC may or may not contain a transmit data buffer.

These last two choices do mean that there are a few different "flavours" of the standard, but the number of possibilities has been kept to a minimum, and most problems arising from them can be avoided by the implementation of (for instance) a digital filter bypass mechanism (whenever a digital filter is provided in the baseband), or a Tx buffer bypass mechanism, so that at expense of a little redundant silicon almost any pair of RF and baseband chips compliant with this specification can be configured to work together.

1.3 Scope

This specification confines its attention to the physical interface between the baseband and the RF IC. It does not prescribe anything within either chip, save for the minimum necessary to ensure compatibility at the physical level. For instance, the serial control interface between baseband and RF IC is assumed to be register-based, but nothing is specified about the address allocation or data length and the interface definition allows great flexibility in this. Similarly, the receive sample interface has extensive configuration options so that the form of the interface does not dictate the implementation of the RF IC receive chain. The intention is to leave chip designers the freedom to seek competitive advantage within the chips, while ensuring that chips compliant with this specification can always work together when correctly configured.

1.4 References

[1] GSM 05.10, Radio Subsystem Synchronisation (section 6.4 in version 7.1.0, or equivalent in later versions)

[2] GSM 05.04, Modulation (section 3.2 in version 8.0.0, or equivalent in later versions)

2 WORKING GROUP AND TERMS

2.1 Working Group

The Working Group consists of representatives of the following companies (in alphabetical order, no priority implied):

Agere Systems
Infineon Technologies
Motorola
Philips Semiconductors
Renesas Technology Corp.
RF Micro Devices
Silicon Laboratories
Sony Semiconductor and Electronic Solutions Division
TTPCom Limited

TTPCom acted as rapporteur for the development and drafting of the standard.

2.2 Terms of Use of this Specification

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The master copy of this document is available on the Web at www.digrf.com from where it may be freely downloaded. Copies or derivatives of this document from any other source are not authoritative. It is the user's responsibility to ensure that they are using the latest version of the standard as a basis for design and implementation.

2.5 Corrections and Improvements

In the event that a user discovers an error in the specification, or has a suggestion for improvement in future versions of the specification, the Working Group would be pleased to be informed. Please email the Rapporteur (Andrew Fogg of TTPCom) at digrf@ttpcom.com .

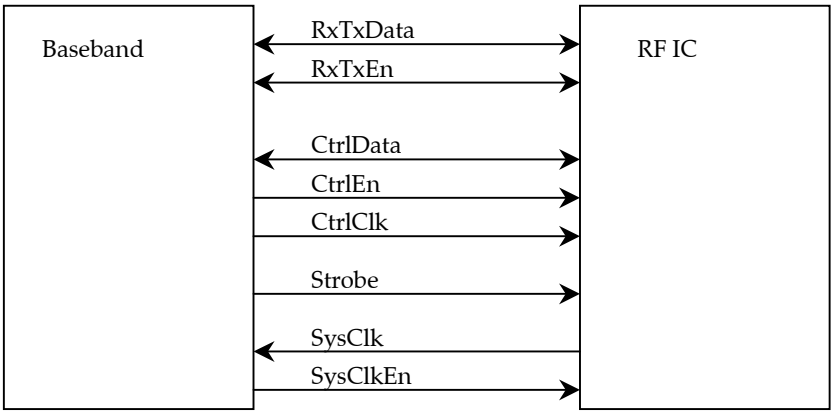
3 INTERFACE OVERVIEW

3.1 Description

The DigRF digital BB / RF Interface is intended to carry:

- transmit symbol information from the baseband to the RF IC
- receive sample information from the RF IC to the baseband
- control information in both directions
- a precise timing signal from the baseband to the RF IC
- system clock from the RF IC to the baseband
- system clock on/off control from the baseband to the RF IC.

There is a strong motivation to minimise the number of IC pins needed to support the interface, especially at the RF IC end, and to that end as many signals are shared or multiplexed as is reasonably feasible. This results in an interface that requires 8 pins, by virtue of multiplexing transmit and receive data (thus restricting the interface to GPRS slot classes 1..12 and 19..29), clocking the data interface off the system clock and using single-ended signals throughout. The only significant further saving that could be achieved would result if multiplexing control and data streams were feasible; this is currently not believed to be possible, and so the interface definition provides a separate control interface. The following block diagram shows the scheme:



Most of the signals, for example the system clock, will require slew rate control to limit the spectrum of the signal to avoid unwanted interference within the RF IC.

3.2 Rx/Tx Data Interface

This interface carries transmit symbol information to the RF IC, which contains GMSK and 8PSK modulators and may also contain a transmit data buffer, and receive IQ sample information in either baseband (post digital filter) or bitstream (raw or prefiltered output from oversampling ADCs, pre digital filter) format. It comprises a data signal and an enable signal and is referred to the system clock for timing.

3.3 Control Interface

This interface carries control information to and from the RF IC. It is a standard 3-wire interface with the baseband as master. For compatibility with other 3-wire-interface devices it includes its own dedicated clock as well as the data and enable lines.

This interface also includes a single strobe signal, typically driven by dedicated hardware in the baseband, which supports precise timing of events within the RF IC.

3.4 Master Clock Interface

This interface provides the system clock to the baseband and a hardware system clock enable line for on/off control of the system clock.

3.5 Interface Configurability

This section gives details of the configuration capabilities and design choices associated with each of the three interfaces. All run-time configuration alternatives are implemented in the baseband; these correspond to fixed design choices in the RF IC. For details of what these options mean, see the relevant parts of Section 4.

Rx/Tx Data Interface: Tx Mode
The RF IC may require Block Mode (there is a TX buffer in RF IC) or Stream mode (no Tx buffer in RF IC). The baseband must support both Block Mode and Stream Mode.

Rx/Tx Data Interface: Rx Mode
The RF IC defines the number of bits per sample and the number of padding bits between samples (and hence implicitly the number of samples per Rx symbol); it is permissible for this to be configured via the Control interface. All RF ICs must support 16 bits per sample at two samples per symbol. RF ICs may optionally provide other combinations of bits per sample and oversampling ratio, for example I/Q 13Msps single-bit bitstreams. The RF IC also sets the I/Q sample order. The location of the digital filter(s) (RF IC or baseband) is a system design choice; see Section 5. Basebands including a digital filter should provide a bypass for the filter; all basebands must accept 16 bits per sample at two samples per

symbol. Basebands may optionally accept other combinations of bits per sample and oversampling ratio. All basebands shall have the capability to accept either order of I/Q sample presentation.

Implementation of 52Mbps mode is optional in both RF IC and baseband.

Rx/Tx Data Interface: both Modes
The RF IC may choose which polarity of SysClk is used for this interface; the baseband must be configurable to accept either polarity. The polarity may be different for Rx and Tx.

Control Interface
The control interface may need to operate with other ICs in the system; it therefore has no configuration options. However, the baseband may vary the CtrlClk frequency depending on operating mode. See Section 4.3.

Master Clock Interface
There are no configuration options on this interface.

4 DETAILED SPECIFICATION

4.1 General Definitions

All logic signals in this interface are active high; that is, a binary 1 in a data stream or the "asserted" state of the signal are represented by a high voltage, and a binary 0 or the "negated" state are represented by a low voltage level.

In some of the timing diagrams in this specification data is shown as being presented on the falling edge of a clock, while in others the clock is shown in the converse polarity; in all cases, the baseband device shall be configurable to match the RF IC device. The RF IC may choose the clock alignment to be used; this may be configurable through a register setting but need not be. The exception to this is the control interface, where for compatibility with other devices the clock polarity is fixed, with data presentation on the falling edge of the clock.

As a general principle, if the clock and data signals in an interface are both driven by the same device, data is presented on one edge of the clock and sampled on the next edge of the opposite polarity, one half clock cycle later, but if the clock and data are driven from opposite ends of the interface, data is presented on one edge of the clock and sampled on the next edge of the same polarity, one full clock cycle later. Note that either may apply depending on the operating mode of some interfaces.

All timings are referred to the signal as observed on the pin of the device driving the signal at the time – note that in a bidirectional interface this means that the timing reference may be on either device depending on operating mode.

All signals in this interface are single-ended (as opposed to differential) and use appropriate logic levels for the process and supply voltage in question (see Section 5.1).

"EMC controlled" means that provision is made to control the rise and fall times of a signal in order to limit its spectral content.

4.2 Rx/Tx Data Interface

4.2.1 RxTxData Signal

This bidirectional signal carries transmit burst symbols (the burst contents prior to modulation) from the baseband to the RF IC during Tx and multiplexed IQ samples from the RF IC to the baseband during Rx. There are two modes of Tx operation (Stream and Block). The single Rx mode includes some framing configuration in the baseband to

accommodate both bitstream input (direct from ΣΔ or similar oversampling converters, digital filter in the baseband) and baseband input (from a digital filter in the RF IC).

The baseband shall initialise RxTxData as an input (since the terminal must receive before it can transmit) and the RF IC shall also initialise RxTxData as an input. Basebands shall provide a weak resistive pulldown to 0V (nominal value 100kΩ) on this signal so that the signal defaults to a negated state when not driven. This signal is EMC controlled.

4.2.2 RxTxEn Signal

The RxTxEn signal is driven by the baseband in Tx mode (Stream and Block) and by the RFIC in Rx mode. In Tx Stream mode basebands must be able to assert RxTxEn to a timing accuracy of one quarter-symbol or better.

Figure 1 shows the timing of assertion of RxTxEn relative to the driving clock edge. The timings for the negation of RxTxEn relative to the driving clock edge are the same.

The baseband shall initialise RxTxEn as an input, and the RF IC shall also initialise RxTxEn as an input. Basebands shall provide a weak resistive pulldown to 0V (nominal value 100kΩ) on this signal.

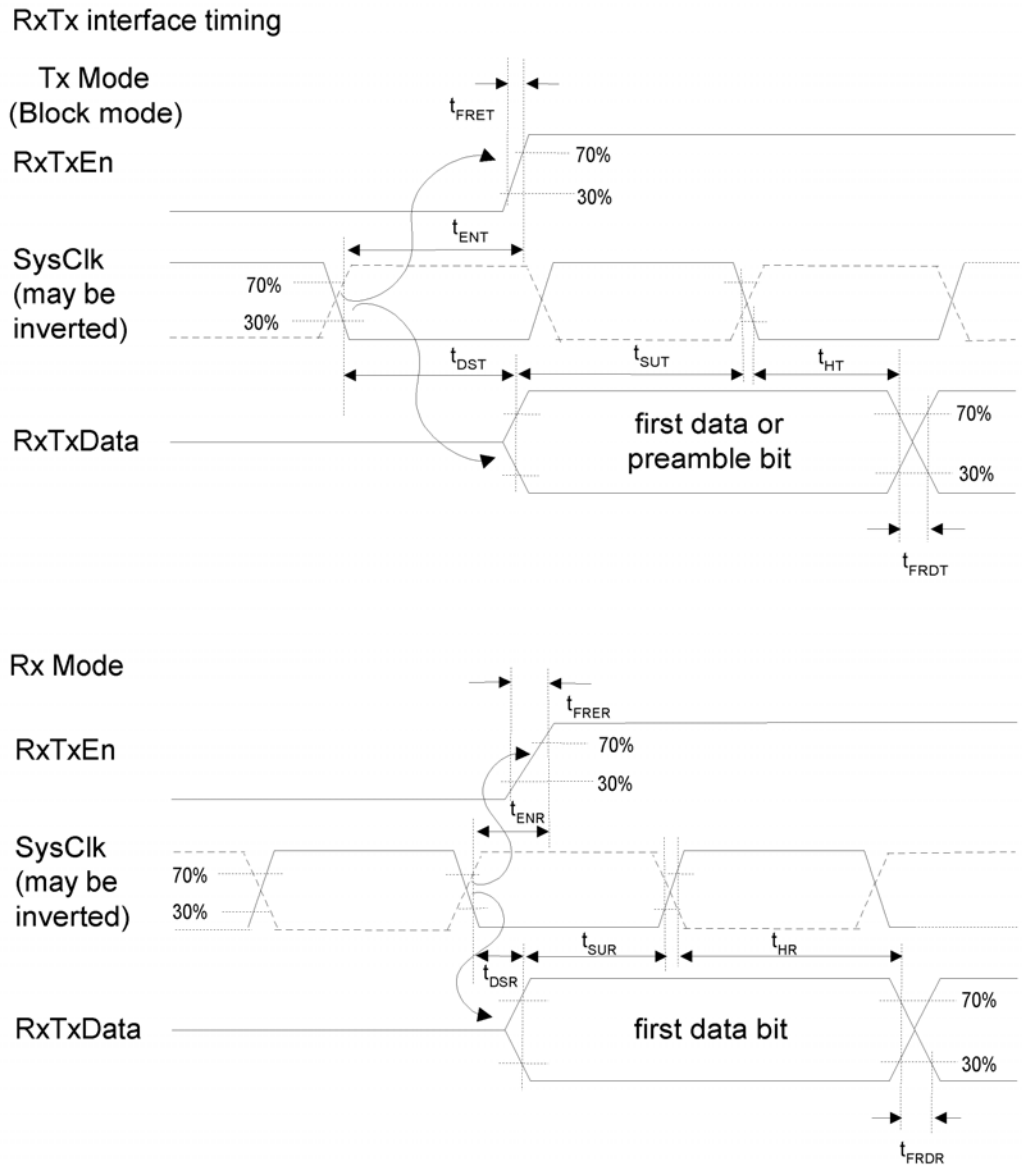


Figure 1: RxTx interface timing

		min	max	unit
Tx mode				
RxTxData fall/rise time	t_{FRDT}	2		ns
RxTxData data stable after driving clock edge	t_{DST}		20	ns
RxTxData (RF IC) input setup requirement	t_{SUT}		6	ns
RxTxData (RF IC) input hold requirement	t_{HT}	0		ns
RxTxEn fall/rise time	t_{FRET}	2		ns
RxTxEn delay from driving clock edge	t_{ENT}		20	ns
Rx mode				
RxTxData fall/rise time	t_{FRDR}	2		ns
RxTxData data stable after driving clock edge	t_{DSR}		10	ns
RxTxData (baseband) input setup requirement	t_{SUR}		3	ns
RxTxData (baseband) input hold requirement	t_{HR}		6	ns
RxTxEn fall/rise time	t_{FRER}	2		ns
RxTxEn delay from driving clock edge	t_{ENR}		10	ns

Table 1: RxTx Interface Timing

The rise and fall times specified in Table 1 are to be met with a nominal load of 10pF.

4.2.3 Tx Stream Mode

TX Stream mode is intended for use when the transmit bit buffer is located in the baseband, so that the modulator in the RF IC has to fetch symbols at symbol rate for modulation. Implementation of Stream mode is mandatory in the baseband IC and optional in the RF IC.

In Tx Stream mode, four data bits per burst symbol are transmitted across the interface at a bit rate of SysClk/24 (so nominally 13MHz/12 or about 1.083Mbps). The data bits are transmitted MSB first. The following truth table indicates the coding of the four bits:

3 MS bits	LS bit	Coding
000	0	GMSK '0'
001	0	GMSK '1'
010	0	proprietary use or GMSK '0' (see text)
011	0	proprietary use or GMSK '1' (see text)
100	0	proprietary use or GMSK '0' (see text)
101	0	proprietary use or GMSK '1' (see text)
110	0	proprietary use or GMSK '0' (see text)
111	0	proprietary use or GMSK '1' (see text)
000…111	1	8PSK symbols, coding of three MSBs as specified in [2]

Table 2: Tx Symbol Bit Coding

The six symbols 0100…1110 may be used for proprietary purposes between basebands and RF ICs that share the same meanings for these combinations. Where the RF IC does not "understand" these bit patterns, the RF IC shall interpret the symbol as a GMSK '0' or '1' according to the third bit of the symbol and ignore the first and second bits. In addition to this the baseband software should refrain from generating these patterns. *Note that in proprietary uses of these six symbols it is not required that the trailing '0' imply GMSK; however, RF ICs not making proprietary use of them shall interpret the trailing '0' in this way, as specified above.*

For the avoidance of doubt, the GMSK symbols represent the burst content prior to differential encoding; differential encoding shall be performed in the GMSK modulator.

The start of transmission is synchronised to the rising edge of RxTxEn line. Transmission shall continue until the symbol buffer in the baseband is empty, with the RFIC simply modulating all symbols provided to it. The RxTxEn line shall be asserted as required by the RF IC during data transfer; note that this may be discontinuously. In this case the minimum gap between assertions is one quarter symbol period.

RF ICs may require and basebands must be able to provide up to 32 preamble symbols immediately before the burst data symbols at the beginning of a transmit event. RF ICs may also require and basebands must be able to provide up to 32 postamble symbols immediately after the burst data symbols at the end of a transmit event. The numbers of preamble and postamble symbols need not be the same; either may be zero. Both are RF IC-specific. The bit coding of the preamble and postamble symbols, unlike the coding of burst data symbols, is RF IC specific. If the RFIC requires preamble symbols the baseband shall supply them immediately preceding the data symbols; if the RFIC requires postamble symbols the baseband shall supply them immediately following the last data symbol.

The baseband shall supply only whole symbols. The baseband shall be capable of supplying up to 32+157+3x156+32 = 689 symbols (to cover four-slot Tx with maximum pre- and postamble), and any number of symbols smaller than this as required by the RFIC for any given transmission. For RFICs operating on a whole-symbol basis the baseband should supply 157 symbols for bursts in timeslots 0 and 4 and 156 symbols for bursts in all other timeslots. For RFICs modulating 156.25 symbols per burst, the baseband shall supply the integer number of symbols per burst specified by the RFIC, with spacing between bursts (if any) as required by the RF IC. The placement of guard (and in the case of a [P]RACH burst, padding) symbols should take account of the timing advance required for the first data symbol in the stream.

RFICs using Stream mode shall provide and specify a constant group delay from assertion of RxTxEn to the Tx chain outputs.

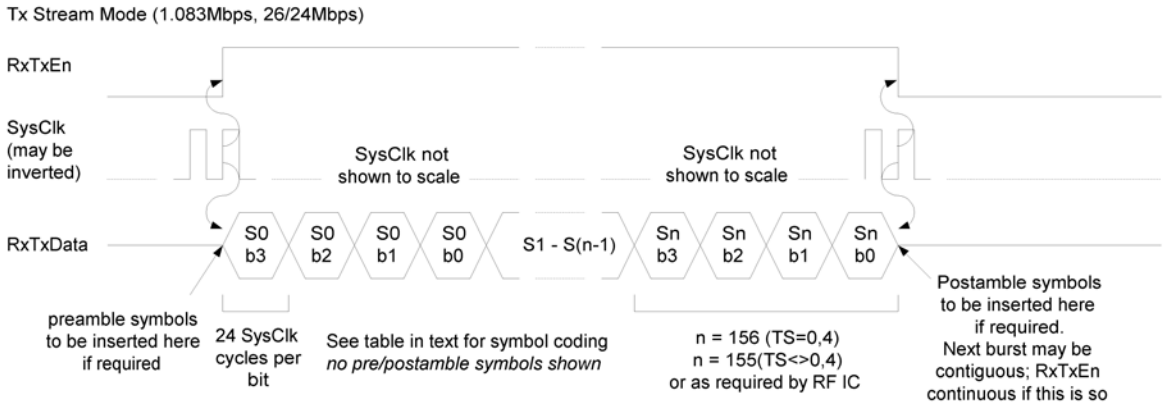


Figure 2: Tx Stream Mode

4.2.4 Tx Block Mode

In Tx Block Mode the burst data bits are transmitted discontinuously at a higher rate, to be held in a buffer in the RF IC ready for modulation. (The idea is to upload while the RF IC is idle, to avoid interference.) The same symbol coding and rules on number of symbols per burst as for Stream mode apply, as does the guard symbol placement, RACH burst coding and preamble/postamble provision. Implementation of Block mode is mandatory in the baseband IC and optional in the RF IC.

RxTxData coding and RxTxEn timing are as for Stream mode, with 4 bits per symbol as before, but the data rate is 26Mbps. Data transfer is synchronised to the rising edge of RxTxEn and continues until the proper number of symbols has been transferred, framed by RxTxEn as before. For multi-slot transmission, if the slot data is sent contiguously, RxTxEn shall remain continuously asserted; if the slot data is discontinuous, there shall be a gap between each burst of a minimum of two SysClk cycles and RxTxEn shall be driven as if the bursts had been widely separated. Basebands shall transfer Tx data in the manner specified by the RF IC. Note that in Block mode the RF IC will need information on how many symbols are to be transmitted; this may be via events on the Strobe line, via registers in the Control interface, use of preamble symbols, by counting the symbols into the buffer, or a combination of these.

RFICs using Block mode shall provide and specify a constant group delay from assertion of Strobe (or from the control interface write triggering transmit, if that is mechanism used by the RF IC) to the Tx chain outputs.

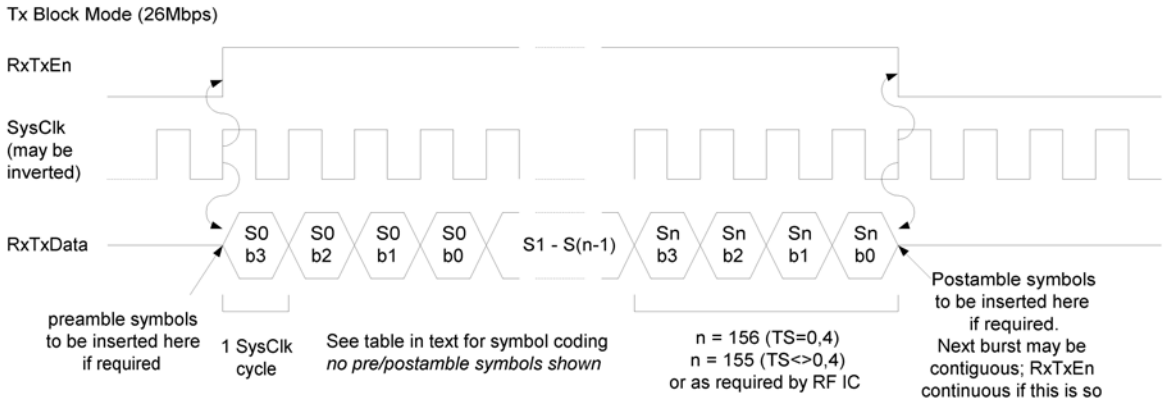


Figure 3: Tx Block Mode

4.2.5 Rx Mode

In Rx Mode, RxTxData carries the sample data from the RF IC to the baseband. IQ information is multiplexed into the same signal. The bit rate is fixed at 26Mbps. To accommodate both bitstream and baseband sample transfer, several parameters may be chosen by the RF IC and configured in the baseband (only):

Bits per sample
The number of data bits per I sample (and thus also per Q sample) may be set at design time to any integer value in the range 1 to 24. The smaller values will be used for ΣΔ (bitstream) outputs, while for digital filter (baseband) outputs a value of 16 is typically used to conform to DSP word sizing. Not all 16 bits are necessarily significant in this case. Support for 16 bits per sample is mandatory in RF ICs containing a digital filter and all basebands; support for other values is optional at both ends of the interface. The ability to use up to 24 bits per sample is provided to allow for possible future ΣΔ converters operating at higher oversampling ratios and providing greater dynamic range. Software should ensure that the bits per sample setting is appropriate to the RF IC in use; incorrect settings will produce invalid data. Samples are transmitted MSB first.

Number of padding bits
For some combinations of bits per sample and sample rate, the I and Q samples will not occupy every cycle of the 26MHz clock. The samples will need to be padded with extra bits to create a continuous stream. The number of pad bits per IQ sample pair should be set to the appropriate integer in the range 0 to 64 for the number of bits per sample and the oversampling ratio. 0 would be appropriate for single-bit input with samples at 13MHz, or for continuous 24-bit samples at two per symbol, or for continuous 12-bit samples at 4 per symbol; 16 would be correct for two 16-bit samples per symbol; 64 is needed for 16-bit samples at one per symbol. Other combinations (for example, for multi-

bit ΣΔs) are possible and permitted. RF ICs containing a digital filter and all basebands must support two samples per symbol; other oversampling ratios are optional. (Basebands whose algorithms are configured for one sample per symbol should accept two samples per symbol over the interface and implement a suitable decimation filter in the DSP.) Incorrect combinations may produce unpredictable (and certainly incorrect) sample acquisition. The polarity of the padding bits is RFIC specific.

IQ order
The I and Q samples are transmitted consecutively. To allow for high- and low-side LOs in different radios, the baseband shall be configurable to route the first sample of each pair to the I buffer and the second to the Q buffer, or vice versa. Assuming I sample first, the bit sequence is [I sample bits][Q sample bits][blank bits, if any], repeated as necessary, *not* [I][blank/2][Q][blank/2].

Some ADC solutions may send two streams of single-bit data at 2 x 26Mbps for processing by a digital filter located in the baseband IC. RF ICs that do this and baseband ICs that accept it shall transfer data using the RxTxData line for the I samples and the RxTxEn line for the Q samples (no framing is needed in this case). Implementation of 52MHz capability is optional, but if it is implemented it shall comply with the timing diagram given below.

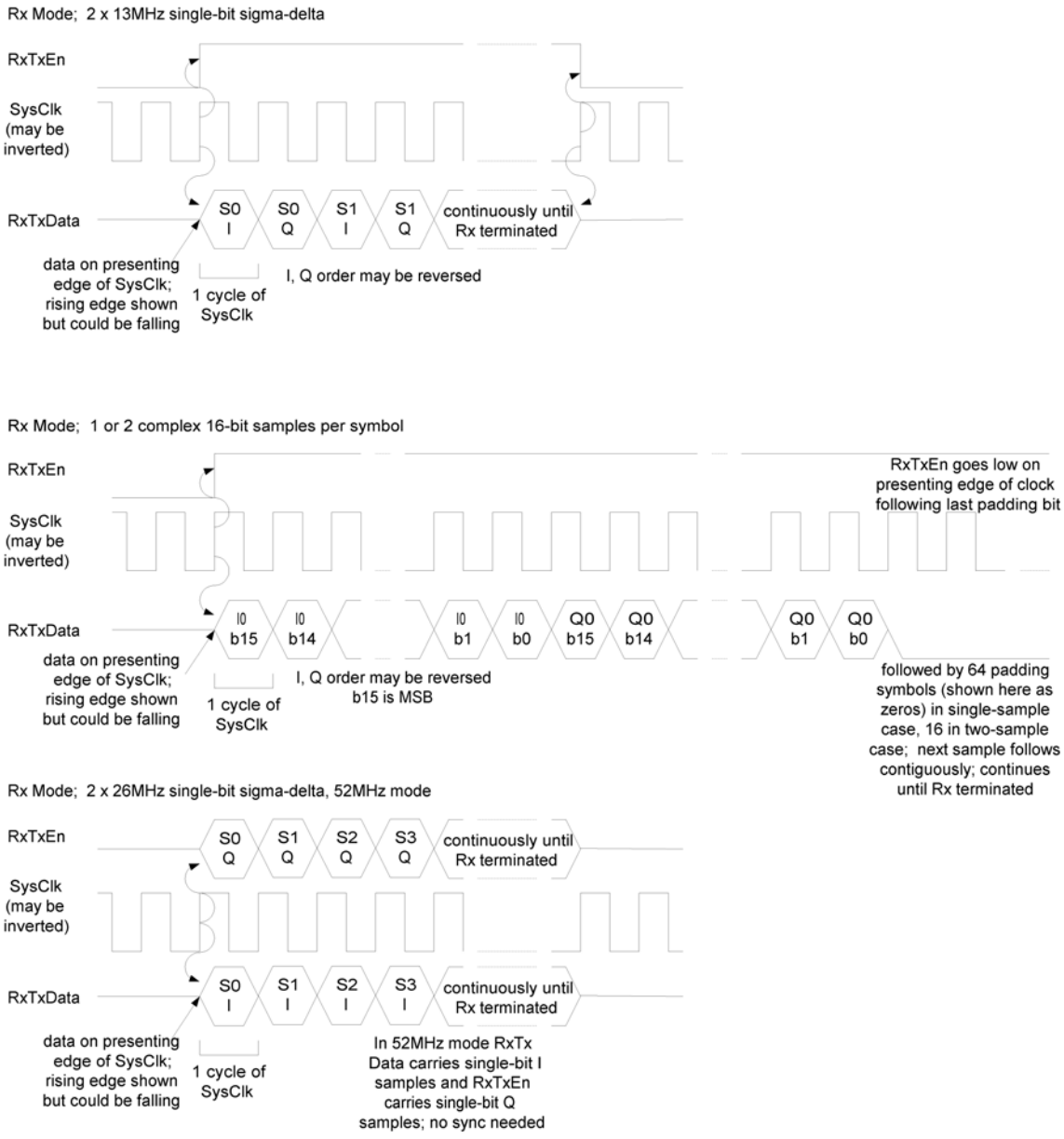


Figure 4: Rx Mode, three examples

In Rx Mode RxTxEn is output by the RFIC and provides a framing signal aligned to the presenting edge of SysClk. The first bit of the first sample from the RF IC (which may be I or Q depending on configuration) is clocked out by the same presentation edge of SysClk as that asserting RxTxEn. Following this the baseband is responsible for maintaining sample, blank and I/Q sync according to the prevailing Rx format configuration. RxTxEn

is negated on the presenting edge of SysClk at the end of the last bit transmitted. See Section 4.2.2 for timing details of the RxTxEn signal.

In Rx mode all RF ICs shall provide and specify a constant time delay from assertion of the Strobe signal (or from the control interface write triggering Rx, if that is the mechanism used) to assertion of RxTxEn, and shall also provide and specify a constant group delay through the Rx chain.

4.2.6 Reference Clock

The reference clock for all transfers over the RxTx Data Interface is the SysClk signal output by the RF IC.

4.3 Control Interface

The control interface provides a bidirectional 3-wire interface accessing the RF IC register set. This standard does not define the number or functions of the registers in the RF IC, and constrains their definition only by limiting the maximum number of bits (including the Read bit and address bits) in any telegram to 32. The interface may be shared with other devices by re-using the CtrlData and CtrlClk signals and generating a separate CtrlEn for each further device.

EMC control on the signals in this interface is not required. *This is to allow for the difficulty of maintaining correct rise and fall times when the load capacitance could vary greatly between systems, depending on the number of devices connected to this bus.*

4.3.1 CtrlData Signal

The CtrlData signal carries the physical content of a control telegram; the Read bit, address bits and data bits. The Read and address bits are always output from the baseband; the data bits may be output from either the baseband (write operation) or the RF IC (read operation). The Read bit is set to 1 for a read operation and 0 for a write operation.

To ensure physical compatibility of the interface, it is required that all transactions are initiated by the baseband transmitting the Read bit first, followed by the proper number of address bits for the RF IC in use and the register addressed, followed by transmission of the data bits in the appropriate direction. Address and data portions of all telegrams are sent MSB first. *Note that this standard does not specify the number of address or data bits required by a particular RFIC, and in fact either may vary even between registers within one RFIC.*

Software in the baseband is responsible for providing the correct number of address bits for the RF IC and register in use, for providing (or reading) the correct number of data bits thereafter for the addressed register, and for providing the correct number of cycles of CtrlClk. Hardware support for this is baseband-specific. The maximum permitted total length of a telegram (sum of number of address bits and number of data bits plus one for the Read bit) is 32 bits. *Note that in the case of a read operation this will result in a full-length telegram requiring 35 cycles of CtrlClk in total, while a full-length write will require 33 cycles.*

The RF IC shall configure the CtrlData pin as an input during initialisation and shall only drive the CtrlData pin as an output during the data portion of a read operation. The baseband shall provide a weak resistive pulldown to 0V (nominal 100kΩ) on this signal.

		min	max	unit
CtrlData Signal				
CtrlData stable after driving clock edge, write operation	t_{DSW}		10	ns
CtrlData input (RF IC) setup requirement, write	t_{SUW}	3		ns
CtrlData input (RF IC) hold requirement, write	t_{HW}	3		ns
CtrlData stable after driving clock edge, read operation	t_{DSR}		20	ns
CtrlData input (RF IC or BB) setup requirement, read	t_{SUR}	3		ns
CtrlData input (RF IC or BB) hold requirement, read	t_{HR}	3		ns
CtrlEn assertion/negation from driving clock edge	t_{EN}		10	ns
RF IC CtrlData output to tristate (input) time (from assertion of CtrlEn by BB – read abort – not shown in Fig 5)	t_{OT}		12	ns

Table 3: CtrlData Signal Timing

Refer to Figure 5 for an illustration of the interpretation of t_{DSx}, t_{SUx} and t_{Hx}. The rise and fall times given in Table 3 shall be achieved with a nominal load of 10pF.

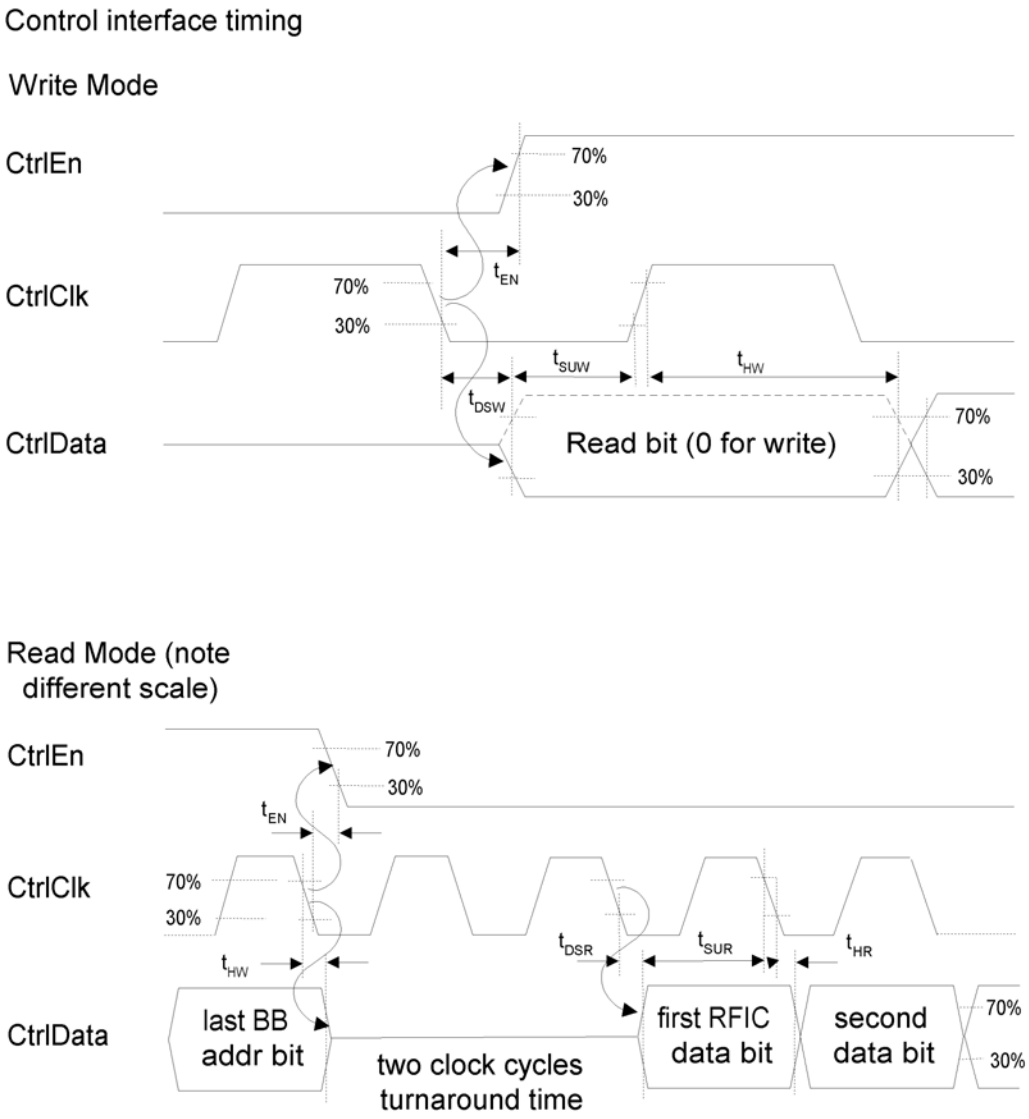


Figure 5: Control Interface Timing

4.3.2 CtrlEn Signal

The CtrlEn signal is used to signal the start and end of the entire telegram in write operations and the address portion in read operations. The Read bit is clocked out of the baseband by the falling edge of CtrlClk that drove assertion of CtrlEn, followed by the appropriate number of address bits. In a write operation the proper number of data bits follows immediately (driven by the baseband) and CtrlEn is negated by the falling edge of CtrlClk during the final data bit. In a read operation, the CtrlEn signal is negated on the falling edge of CtrlClk during the last address bit, and the RF IC should present the

requested data starting on the second falling edge of CtrlClk after CtrlEn goes low, giving two cycles of CtrlClk for the RF IC to access the addressed register and present the data.

If CtrlEn is asserted during the data portion of a read operation the RF IC shall immediately configure the CtrlData line as an input and begin a new write operation. The baseband shall always assert CtrlEn in proper timing (clock edge) alignment to CtrlClk.

There shall be a minimum of two periods of the currently-selected CtrlClk frequency between successive telegrams on the Ctrl interface during which time CtrlEn shall be negated using the normal timing relationship. The RF IC shall latch data written to it by the end of these two clock cycles. Basebands must be capable of asserting CtrlEn to an accuracy of one quarter symbol period or better for the purposes of triggering Rx operations and Tx Block mode operations, to accommodate RF ICs that require this.

CtrlEn Signal		min	max	
delay from driving clock edge	t_{EN}		10	ns

Table 4: CtrlEn signal timing

See Figure 5 and Table 4 for timing details of CtrlEn.

If the interface is shared with other devices, each device shall have a dedicated CtrlEn signal to act as a device select line.

CtrlEn shall be driven low on reset.

4.3.3 CtrlClk Signal

The CtrlClk signal is output from the baseband while the Control Interface is active (and not otherwise). If multiple telegrams are being sent consecutively CtrlClk may run continuously between them, observing the inter-telegram gap specified above, but must be turned off after the last one has completed.

The maximum permitted CtrlClk frequency is the same as SysClk (26MHz); CtrlClk need not, but may, be derived from SysClk. RF ICs shall accept any CtrlClk frequency up to the maximum; note that CtrlClk may, or may not, be asynchronous to SysClk. The CtrlClk frequency may vary according to the operating mode of the baseband, but shall not change during any transaction on the interface.

The polarity of CtrlClk shall be data presentation on the falling edge, for compatibility with other devices that may share this interface in some systems. CtrlClk shall be driven low on reset and held low when the Control interface is inactive.

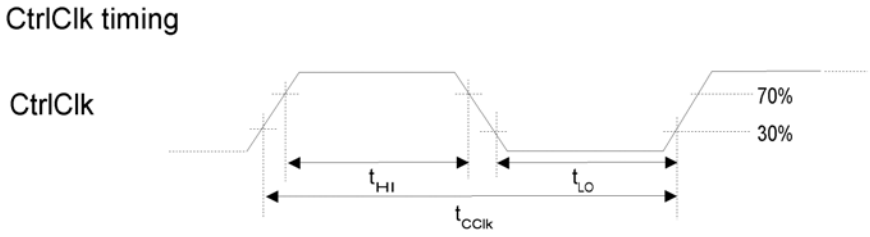


Figure 6: CtrlClk timing

		min	max	unit
CtrlClk timing				
frequency	f_{CClk}		26	MHz
period	t_{CClk}	38.4		ns
high/low time	t_{HI}, t_{LO}	13		ns

Table 5: CtrlClk Timing

The timings given in Table 5 shall be achieved with a nominal load of 10pF.

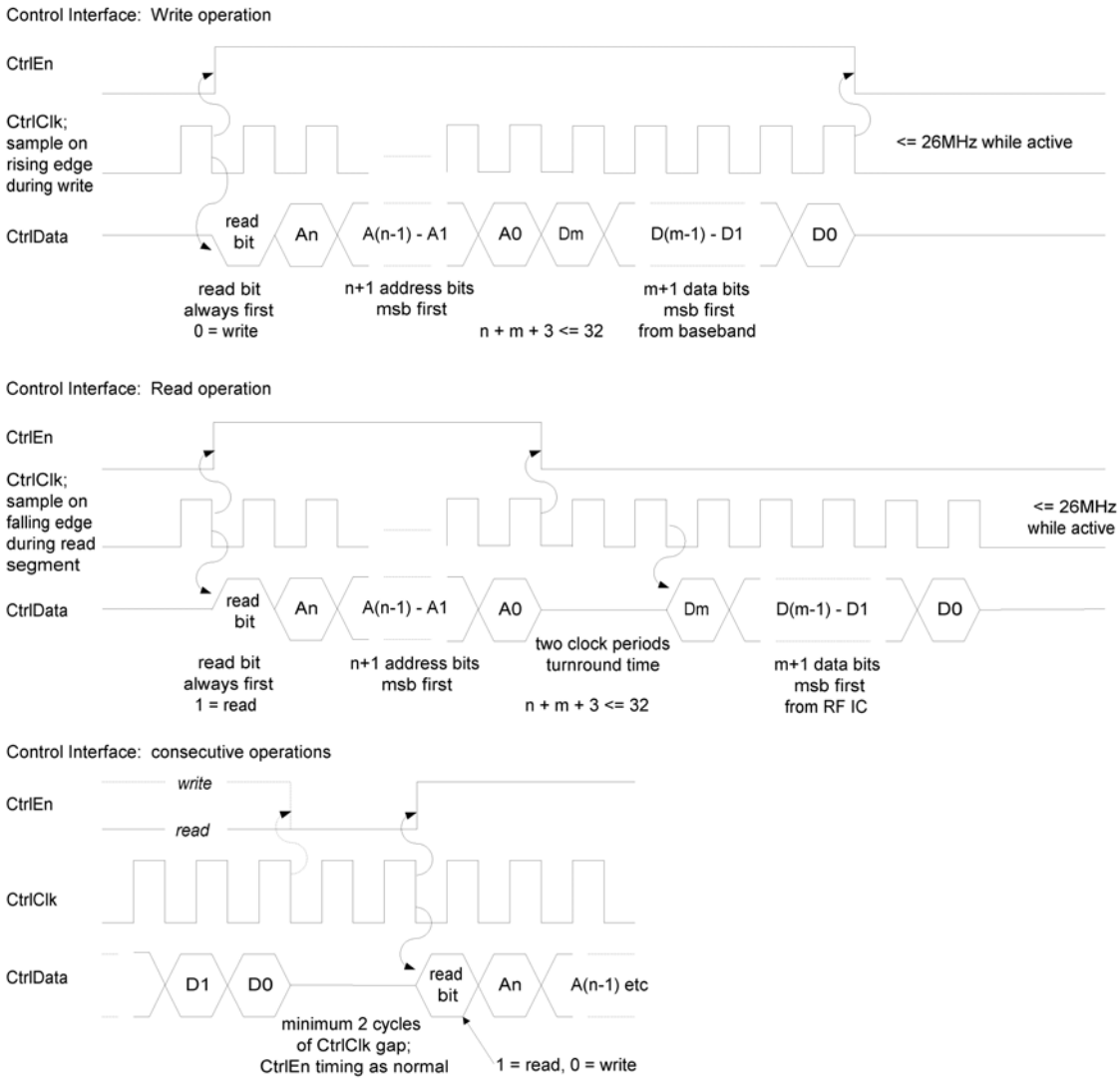


Figure 7: Control interface

4.3.4 Strobe Signal

The Strobe signal is provided to support precise timing of events inside the RF IC. The most obvious example of this is the start of burst modulation and/or power ramping, but the use of the Strobe line is not constrained to these events. The Strobe line is output from the baseband and will typically be generated by timing hardware in the baseband, and may be used as desired to synchronise events within the RF IC. A typical use within the RF IC might be to advance a state machine, or to trigger the next event in an event FIFO. Any necessary programming data for such things is provided via the Control Interface and the RF IC register set.

The Strobe signal is active high, shall be asserted for exactly one quarter-symbol period (so 24 SysClk cycles), and shall be negated thereafter, for a minimum of one quarter-symbol period. Also, the time between Strobe signal assertions shall always be an integer number of quarter-symbol periods. This specification does not constrain how the RF IC detects the Strobe signal; edge or level detection may be used. It is the responsibility of the baseband hardware and software to generate the Strobe signal when required in a manner compatible with the RF IC in use. RF ICs must accept the quarter-symbol granularity of the Strobe signal.

The RF IC shall detect and act on the Strobe signal within two SysClk cycles of assertion.

EMC control is required; the rise and fall times of the signal shall be not less than 2ns. *This is because the Strobe signal will definitely be used while the radio is active (eg to terminate Tx mode).* These times shall be achieved for a nominal load of 10pF.

4.4 Master Clock Interface

4.4.1 SysClk Signal

The SysClk signal is generated by the RF IC while the SysClkEn signal is asserted. It has a nominal frequency of 26.0MHz. This specification does not define the frequency tolerance of the master clock, nor the means by which AFC is applied. (For example, this could be by AFC DAC in the RF IC, AFC DAC in the baseband, or by digital correction of the transmit and receive streams and other timers to take account of the prevailing master clock error.) However, device interfaces conforming to this standard shall work correctly for SysClk frequencies of 26.0MHz plus or minus at least 100ppm.

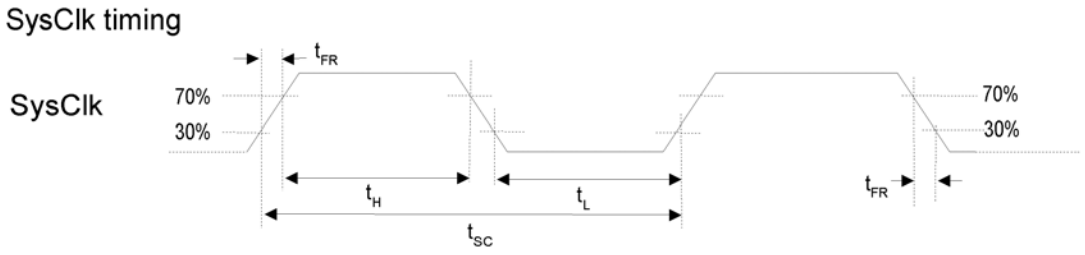


Figure 8: SysClk timing

		min	typ	max	Unit
SysClk timing					
Frequency	f_{SC}		26		MHz
Period	t_{SC}		38.462		ns
Clock high / low time	t_H, t_L	13			ns
fall/rise time	t_{FR}	2			ns

Table 6: SysClk Timing

The SysClk output intended for the baseband IC on the RF IC should be capable of driving at least 10pF while maintaining specification. It is strongly recommended that RF ICs provide a means of driving SysClk to at least one additional device; whether this is achieved by increasing the drive capability of the SysClk output or by providing additional SysClk output pins is implementation-dependent.

4.4.2 SysClkEn Signal

The SysClkEn signal is generated by the baseband. It enables the RF IC 26MHz SysClk output and powers the 26MHz oscillator when asserted. When SysClkEn is negated the 26MHz oscillator shall be halted and the SysClk output shall be held low. Note that there will be an implementation-specific delay from assertion of SysClkEn to SysClk operation within the specified timing parameters.

The SysClkEn signal does not require EMC control.

The SysClkEn output on the baseband should be capable of driving at least two CMOS inputs (at least 20pF) so that it can switch the 26MHz oscillator power directly if this is required as well as drive the SysClkEn input on the RF IC.

5 IMPLEMENTATION ASPECTS

5.1 Logic Levels and Thresholds

In order to ensure compatibility between RF ICs and basebands on different semiconductor processes and having different operating voltages, the signals in the interface, including the SysClk signal, shall comply with the following:

	Notes	**min**	**max**	**unit**
V_{CC}	interface supply voltage	1.5 - 5%	1.8 + 5%	V
Outputs				
V_{OL}	output low voltage, I_{OL} = 500µA		0.2 x V_{CC}	V
V_{OH}	output high voltage, I_{OH} = -500µA	0.8 x V_{CC}		V
Tristate	tristate leakage current		10	µA
Inputs				
V_{IL}	input low voltage	-0.3	0.3 x V_{CC}	V
V_{IH}	input high voltage	0.7 x V_{CC}	V_{CC}+0.3	V
I_{IL}	input current, input = 0V	-10	10	µA
I_{IH}	input current, input = V_{CC}	-10	10	µA
C_{IN}	input capacitance		6	pF
Slew rate	input slew rate	50		V/µs

Table 7: Logic Levels and Thresholds

Notes
Some RF ICs may operate their analog sections at higher supply voltages than this interface specification allows; however, such ICs are typically already provided with a separate supply for their digital sections that will comply with these limits. The actual interface operating voltage shall be set by the baseband; all RF ICs must accept any interface operating voltage within the limits given in the above table.

The timing constraints set out elsewhere in this specification shall be complied with under the full range of conditions given above. The operating temperature range is implementation specific.

5.2 Digital Filter Bypass

Basebands including a digital filter shall provide a selectable means to bypass the filter, accepting multi-bit baseband samples at the baseband input. All basebands shall support, at a minimum, 16-bit samples at two samples per symbol.

5.3 Digital Filter Implementation

The precise implementation of the digital filter is dependent on the analog filtering provided in the RF IC. For this reason it is strongly recommended that digital filters in baseband chips have programmable taps. The number of taps and their resolution may also be affected by whether the radio is NZIF or direct conversion. Implementors should consider these issues when specifying a baseband digital filter; if the filter is in the RF IC, it is of course specific to that radio and should be optimised for it.

5.4 Tx Buffer Mode

Basebands shall implement both Tx Stream Mode and Tx Block Mode to ensure compatibility with all RF ICs.

6 FUTURE DEVELOPMENT

6.1 2.5G

Extension to cover EGPRS slot classes 13..18 and other full-duplex modes and standards (ie those requiring simultaneous receive and transmit) is foreseen should practical demand arise. This would require the receive and transmit data streams to be given separate signals.

6.2 3G

Extension to cover several "flavours" of 3G is likely in due course, including at a minimum UMTS and possibly also other 3G standards. Like EGPRS slot classes 13..18, UMTS would require the transmit and receive streams to be separated.