How You Can Benefit from Using MIPI A-PHY in Your Next Automotive Design

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Valens Semiconductor
MIPI A-PHY Overview

Today: Proprietary Interface Bridge Solutions

Tomorrow: A-PHY Standard Interface Bridge Solutions

Future: Integrated A-PHY

Lower cost through standardization and economies of scale

Lower cost/eBOM through integration

ECU: Electronic Control Unit  SoC: System On Chip
MIPI A-PHY – Automotive Long-Reach PHY

The first industry-standard long-reach asymmetric SerDes physical layer specification targeted for ADAS/ADS surround sensor applications and infotainment display applications

A-PHY v1.0 offers:

- Direct coupling to native CSI-2/DSI-2/DP-eDP protocols
- High performance of up to 16 Gbps over 10-15m
- High noise immunity, ultra low PER (< 10^{-19})
- Supports bridge-based and endpoint integration
- Support for automotive coax and STP\SPP channels
- Power over cable

**NEW** A-PHY v1.1 Enhancements:

- Increased support for lower cost legacy cables
- Double uplink data rate
- Star quad cable support, enabling dual downlink operation

Examples:

Source
Sensor CSI-2
SoC DSI-2
SoC VESA DP

Coax, STP or SPP Cable

Downlink

Examples:

Sink
SoC CSI-2
Display DSI-2
Display DP

Uplink

ADI: Advanced Driver Assistance System
ADS: Autonomous Driving System
SoC: System On Chip
PER: Packet Error Rate
STP: Shielded Twisted Pair
SPP: Shielded Parallel Pair

ADAS:

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A-PHY v1.0 Performance- and Immunity-Based Profiles

Performance Variance and Scalability

• A-PHY scales up the bandwidth without changing the cables and connectors by increasing the PAM level

Noise Immunity (EMC RF Ingress) Variance

• Different OEMs have different requirements
• MIPI-conducted EMC tests at independent labs evaluating noise levels and shielding effects degradation after mechanical stress and aging

Two Performance / Noise Immunity Profiles

• Profile 1: Optimized for low cost/power implementations for lower gears with lower noise immunity and target PER <10^9
• Profile 2: Optimized for Vehicle Life-span, link robustness for all Gears with high noise immunity and target PER <10^{-19}

Interoperability

• Full inter-profile interoperability
• A-PHY Device supporting Gear N (N could be 1–5) shall support all lower gears.

MIPI A-PHY v1.0 Performance

<table>
<thead>
<tr>
<th>Downlink Gear Data Rate</th>
<th>Modulation</th>
<th>Modulation Bandwidth (GHz)</th>
<th>Max Net App Data Rate (Gbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>G1 2 Gbps</td>
<td>NRZ-8B/10B</td>
<td>1</td>
<td>1.5</td>
</tr>
<tr>
<td>G2 4 Gbps</td>
<td>NRZ-8B/10B</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>G3 8 Gbps</td>
<td>PAM4</td>
<td>2</td>
<td>7.2</td>
</tr>
<tr>
<td>G4 12 Gbps</td>
<td>PAM8</td>
<td>2</td>
<td>10.8</td>
</tr>
<tr>
<td>G5 16 Gbps</td>
<td>PAM16</td>
<td>2</td>
<td>14.4</td>
</tr>
<tr>
<td>Uplink 100Mbps</td>
<td>NRZ-8B/10B</td>
<td>0.05</td>
<td>55 Mbps</td>
</tr>
</tbody>
</table>
What Makes MIPI A-PHY So Robust and Efficient?

**RTS + NBIC**

- **Time bounded local PHY level retransmission**
  - Only within pre-defined “Overall Delay” (~6μs@G5)
  - Local: Transparent to the upper layers
  - Local: Happens within a single A-PHY hop

- **Dynamic modulation for retransmitted packets with better error resistance**

- **Highly Resilient**
  - Overcomes large Thousands symbols-long error bursts
  - Multiple 10s mV, instantly attacking NBI peaks

- **High Reliability → PER < 10^{-19}**

- **Low Overhead → 90% Net Data Rate**

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**Abbreviations:***

- RTS: Re-Transmission Sub-Layer
- NBIC: Narrow Band Interferences Canceller
- PMD: Physical Media Dependent
- PCS: Physical Coding Sub-Layer
- NBI: Narrow Band Interferences

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[Diagram of MIPI A-PHY protocol layers and retransmission sub-layer with adaptations for various scenarios.]
A-Packet

- The A-Packet is structured to carry Native Protocol data and all information that the A-PHY Data Link Layer requires to perform its functions efficiently
- Downlink and uplink use the same packet structure
- Structure is optimized, supporting aggregation of multiple protocols with minimal overhead and latency
- A-Packet header contains all required information (e.g., QoS, Priority, Destination, Protocol Type)
- The A-Packet structure:
  - Header - 8 Byte including MC (Message Counter)
  - Payload
  - Tail – 4 Byte (CRC-32)
A-PHY Interconnect

- A-PHY is a single lane, point-to-point, serial communication technology
- Support for multiple cable types – SDP/Coax
- Power over cable supported
- Up to 15m with 4 inline connectors
A-PHY Functional Safety Features

- A-PHY packets are end-to-end protected as recommended in ISO-26262:2018:
  - CRC-32 for each packet, providing a Hamming-Distance of more than 3
  - Message Counter that is 8 bits wide
  - Timeout monitoring is fulfilled by the Keep-Alive function
- The above measures are necessary to argue a high diagnostic coverage for a communication bus, per Table D.6 in ISO 26262-5:2018
- All other functional safety features necessary to fulfill the required system-level safety goal with ASIL are expected to be managed by upper layers

A-PHY’s tunnels, end-to-end, all the protection elements, allowing both Safety and Security (SPDM).
What’s Coming in A-PHY v1.1

A-PHY v1.1 enhancements:
- 200 Mbps double rate uplink (U2)
- Optional PAM4 modes for G1 & G2
- Adds STQ cable support (see next slide)

Enhanced Performance Variance and Scalability
Expands PAM4 encoding to lower gears, reducing the operating signal rate of these gears and allowing implementation of A-PHY using lower cost legacy cables and connectors.

Same High Noise Immunity (EMC RF Ingress)
Supports same high noise immunity with an ultra-low Packet Error Rate ($< 10^{-19}$) built for vehicle life span support

Interoperability and Compatibility
- A-PHY v1.1 backward compatible with v1.0
- A-PHY v1.0 forward compatible with v1.1

A-PHY guarantees full inter-profile interoperability; devices will support all the various gears below them

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<td>1</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td>PAM4 (Optional)</td>
<td>0.5</td>
<td>1.8</td>
</tr>
<tr>
<td>G2</td>
<td>NRZ-8B/10B</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>PAM4 (Optional)</td>
<td>1</td>
<td>3.6</td>
</tr>
<tr>
<td>G3</td>
<td>PAM4</td>
<td>2</td>
<td>7.2</td>
</tr>
<tr>
<td>G4</td>
<td>PAM8</td>
<td>2</td>
<td>10.8</td>
</tr>
<tr>
<td>G5</td>
<td>PAM16</td>
<td>2</td>
<td>14.4</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Uplink Gear Data Rate</th>
<th>Modulation</th>
<th>Modulation Bandwidth (MHz)</th>
<th>Max Net App Data Rate (Mbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1</td>
<td>NRZ-8B/10B</td>
<td>50</td>
<td>55</td>
</tr>
<tr>
<td>U2</td>
<td>PAM4-8B/10B</td>
<td>50</td>
<td>125</td>
</tr>
</tbody>
</table>
A-PHY v1.1: Adds Support for STQ Cables

- Supports Star Quad (STQ) shielded dual differential pair (i.e., 4 conductor) cables and High-Speed Data (HSD) connectors.
- Referred to as “Q-Port” within the A-PHY working group.
- Efficient size, cost and weight compared to two separate Shielded Differential Pair (SDP) cables.

### A-PHY v1.1 STQ Cable Configuration Examples

<table>
<thead>
<tr>
<th>Example 1: Dual Downlink Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Up to 32 Gbps Downlink</td>
</tr>
<tr>
<td>100/200 Mbps Uplink</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Example 2: Asymmetric Configuration</td>
</tr>
<tr>
<td>Up to 16 Gbps Downlink</td>
</tr>
<tr>
<td>Up to 4 Gbps Reverse Downlink</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Example 3: Symmetric Configuration</td>
</tr>
<tr>
<td>Up to 16 Gbps Downlink</td>
</tr>
<tr>
<td>Up to 16 Gbps Reverse Downlink</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Source</th>
<th>STQ Cable</th>
<th>Sink</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Pair#0: G5 – 16 Gbps Downlink &amp; U1/2 Uplink</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pair#1: G5 - 16 Gbps Downlink</td>
<td></td>
</tr>
</tbody>
</table>

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<td></td>
<td>Pair#0: G5 – 16 Gbps Downlink</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pair#1: G2 – 4 Gbps Reverse Downlink</td>
<td></td>
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</tbody>
</table>
A-PHY is the Foundation of MIPI Automotive SerDes Solutions (MASS)

- Direct coupling to native MIPI protocols (i.e., CSI-2, DSI-2)
- End to End Functional Safety
- End to End Security (WIP)
- Multiple supporting interfaces:
  - I2C
  - GPIO
  - Ethernet
  - MIPI I3C (WIP)
  - SPI (WIP)
First MIPI A-PHY Compliant Chipset – Available

- MIPI A-PHY V1.0 compliant system
- Up to 8Gbps Downlink (G1-G3)
- ISO-26262, ASIL-B
- Serializer
  - CSI-2 input over D-PHY
  - 4 Data Lanes up to 2.5Gbps per lane
  - 16 Virtual Channels
  - Control – I2C, GPIO
- Quad De-serializer
  - 4 x A-PHY Ports (G3)
  - 2 x CSI-2 output over D/C-PHY
  - D-PHY - 4 Data Lanes up to 2.5Gbps per lane
  - C-PHY – 2 Data Lanes up to 5.7 Gsps per lane
  - Control – I2C, GPIO
Example Use Cases
Use Case I - Surround View

Direct coupling to native CSI-2 and control interfaces
End Point integration – Cost and power reduction
Power Over Cable Support up to 6W

High performance of up to 16 Gbps over 15m
High noise immunity
Ultra low PER $< 10^{-19}$

Backward/Forward compatibility
Easy installation and maintenance – self adapting
Use Case II – Display Cockpit

<table>
<thead>
<tr>
<th>Display Type</th>
<th>Number</th>
<th>Size (Inches)</th>
<th>Example Resolution</th>
<th>Net Data Throughput (Gbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Driver Instrument Display</td>
<td>1</td>
<td>12.3</td>
<td>3840x1440</td>
<td>8.4</td>
</tr>
<tr>
<td>2 Center Information Display</td>
<td>1</td>
<td>12.3</td>
<td>3840x2160</td>
<td>12.6</td>
</tr>
<tr>
<td>3 Lower Control Display</td>
<td>1</td>
<td>12.4</td>
<td>3840x2160</td>
<td>12.6</td>
</tr>
<tr>
<td>4 Co-Driver Display</td>
<td>1</td>
<td>12.3</td>
<td>3840x2160</td>
<td>12.6</td>
</tr>
<tr>
<td>5 Side Digital-Mirror Displays</td>
<td>2</td>
<td>7</td>
<td>1280x800</td>
<td>1.5</td>
</tr>
<tr>
<td>6 Heads-Up Display</td>
<td>1</td>
<td>3.1</td>
<td>850x480</td>
<td>0.6</td>
</tr>
<tr>
<td>7 Rear Seat Entertainment</td>
<td>2+</td>
<td>12.5</td>
<td>3820x2160</td>
<td>12.6</td>
</tr>
<tr>
<td>8 Rear Digital-Mirror Display</td>
<td>1</td>
<td>9.7</td>
<td>1280x320</td>
<td>0.75</td>
</tr>
</tbody>
</table>

Notes

- Bandwidth calculation assumes 24b@60Hz VESA CVT 1.2 timing
- VESA DSC Compression can be applied with no additional overhead – can support links of up to 48Gbps (~43Gbps net data)
- A-PHY V1.1 Dual Downlink (32Gbps) with compression can support up to 96Gbps (~86Gbps net data).
- A-PHY V1.1 provides flexibility for the return channel
Use Case II – Display Cockpit

**Instrument Cluster**
- Functional Safety
- Ultra Low PER

**Infotainment Cluster**
- Daisy Chain topology support
- Ultra low PER enables use of compression with no additional overhead
- High Bandwidth of 16Gbps and higher when implementing compression

- Up to 15m
- Multiple protocols:
  - DisplayPort
  - DSI-2
- HDCP Support
Summary

- **Established ecosystem with multiple vendors working on A-PHY compliant chipsets**
  - First samples will be available by EOY2021
- **Clear and forward-looking roadmap and planning**
  - A-PHY v1.0 - Released in 2020
  - A-PHY v1.1 - Targeted for release in 2021
  - A-PHY v2.0 - Work has started in the MIPI A-PHY Working Group
  - New PALs - Expanding support for command-and-control interfaces, such as SPI and Ethernet
- **Supporting multiple advanced use cases with clear advantages of an industry standard**
  - “Error Free” links
  - Seamless integration
  - Interoperability and forward compatibility
MIPI Automotive Resources

Information on A-PHY can be found at:

- MIPI A-PHY Specification Homepage
- MIPI White Paper: Introduction to MASS
MIPI Automotive Workshop

An in-depth look at the MIPI Automotive SerDes Solutions (MASS) framework

Q&A