Alain Legault
Hardent
Create Higher Resolution Displays With VESA Display Stream Compression
What Is VESA DSC?
Why Is VESA DSC Needed?

Mobile application processor
Computer GPU card
Car application processor
MIPI DSI℠
DisplayPort cable
Proprietary transport
DDIC
Computer monitor
Car infotainment display
Display Resolution Growth

Display Vs Link Bandwidth (Gbps)

10x / 5 years
3x / 5 years

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VESPA DSC Block Diagram

Source: VESA DSC white paper
VES A DSC Algorithm

• Intra-frame Constant Bit Rate (CBR) encoder
• Based on Delta Pulse Code Modulation (DPCM)
• Mid Point (MPP), Block Predictor (BP)
• Modified Median Adaptive Predictor (MMAP)
• Indexed Color History (ICH)
• Requires a single line of pixel storage + rate buffer
  – Ultra-low latency
• Visually lossless compression between 2x – 3x
• Video quality excellent with all types of content
  – Natural and test images, text, and graphics
### PHY Speed / Display Resolution

#### MIPI D-PHY℠ v1.1 1.5 Gbps / lane

<table>
<thead>
<tr>
<th>Resolution</th>
<th>FHD (1080x1920)</th>
<th>WQHD (1440x2560)</th>
<th>WQXGA (1600x2560)</th>
<th>UHD (2160x3840)</th>
<th>WQUXGA (2400x3840)</th>
<th>5K (2880x5120)</th>
<th>8K (4320x8192)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>3.58Gbps</td>
<td>6.37Gbps</td>
<td>7.08Gbps</td>
<td>14.33Gbps</td>
<td>15.93Gbps</td>
<td>25.49Gbps</td>
<td>61.16Gbps</td>
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<tr>
<td>No compression</td>
<td>3 lanes</td>
<td>6 or 8 lanes</td>
<td>6 or 8 lanes</td>
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<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
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<tr>
<td>2x compression</td>
<td>2 lanes</td>
<td>3 lanes</td>
<td>3 lanes</td>
<td>8 or 6 lanes</td>
<td>8 or 6 lanes</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>3x compression</td>
<td>1 lane</td>
<td>2 lanes</td>
<td>2 lanes</td>
<td>4 lanes</td>
<td>4 lanes</td>
<td>8 lanes</td>
<td>N/A</td>
</tr>
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</table>

#### MIPI D-PHY v1.2 2.5 Gbps / lane

<table>
<thead>
<tr>
<th>Resolution</th>
<th>FHD (1080x1920)</th>
<th>WQHD (1440x2560)</th>
<th>WQXGA (1600x2560)</th>
<th>UHD (2160x3840)</th>
<th>WQUXGA (2400x3840)</th>
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<th>8K (4320x8192)</th>
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<tr>
<td>Bandwidth</td>
<td>3.58Gbps</td>
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<td>14.33Gbps</td>
<td>15.93Gbps</td>
<td>25.49Gbps</td>
<td>61.16Gbps</td>
</tr>
<tr>
<td>No compression</td>
<td>2 lanes</td>
<td>3 lanes</td>
<td>3 lanes</td>
<td>8 or 6 lanes</td>
<td>8 lanes</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>2x compression</td>
<td>1 lane</td>
<td>2 lanes</td>
<td>2 lanes</td>
<td>3 lanes</td>
<td>4 lanes</td>
<td>8 or 6 lanes</td>
<td>N/A</td>
</tr>
<tr>
<td>3x compression</td>
<td>1 lane</td>
<td>1 lane</td>
<td>1 lane</td>
<td>2 lanes</td>
<td>3 lanes</td>
<td>4 lanes</td>
<td>N/A</td>
</tr>
</tbody>
</table>
MIPI DSI Link Compression

Video In

Processor

TX Port

DSC Encoder

GPU

Display Module

RX Port

Frame Buffer

DSC Decoder

To Display

To Display Video In Processor TX Port DSC Encoder GPU Display Module RX Port Frame Buffer DSC Decoder To Display
# VESA DSC Standard Availability and Support

<table>
<thead>
<tr>
<th>Feature</th>
<th>DSC 1.1</th>
<th>DSC 1.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intraframe coding for images and video</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Visually lossless performance verified by subjective testing</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Detailed standard description</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Normative encoder and normative decoder</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Normative C language code and WIN32 binary</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>High Dynamic Range (HDR)/Wide Color Gamut (WCG)-ready</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>8, 10, 12 bits per color support</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>14 and 16 bits per color support</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>RGB and YCbCr 4:4:4 native coding</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>YCbCr 4:2:2 native coding</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>YCbCr 4:2:0 native coding</td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>

Source: VESA
Transport Standards Using VESA DSC

- MIPI DSI 1.2
- eDisplayPort 1.4b
- DisplayPort 1.4
- HDMI 2.1
Why Adopt VESA DSC?

• Visually lossless picture quality for all content
  – Photos, videos, text, graphics, and test patterns
• Increases data transport capacity by up to 3X
• Compatible with major transport standards
  – MIPI DSI, DisplayPort 1.4, HDMI 2.1
• Ultra-low latency
• Scalable display resolution, frame rate, and colour depth
  – Up to 8K @ 120Hz with HDR
• Reduces power consumption, system costs, and EMI
DSC Helps Save Power, Area, and Cost

Application Processor
- DSC Encoder
- MIPI DSI Tx

MIPI DSI Transport Lanes

Display Driver IC
- MIPI DSI Rx
- MIPI DSI Tx
- DSC Decoder

Frame Buffer
- SDRAM

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DSC Helps Save Power, Area, and Cost

Application Processor

MIPI DSI Tx
DSC Encoder

MIPI DSI Tx

Display Driver IC

MIPI DSI Rx
DSC Decoder

MIPI DSI Rx

Remove
MIPI Tx + PHY
MIPI Rx + PHY

SDRAM

Frame Buffer
DSC Helps Save Power, Area, and Cost

Application Processor

DSC Encoder

MIPI DSI Tx

Display Driver IC

DSC Decoder

MIPI DSI Rx

Remove SDRAMs

Frame Buffer

SDRAM

SDRAM

Frame Buffer

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DSC Helps Save Power, Area, and Cost

Application Processor

MIPI DSI Tx

MIPI DSI Transport Lanes

MIPI DSI Rx

Display Driver IC

DSC Encoder

DSC Decoder

SDRAM

Frame Buffer

Less power
Smaller footprint
Lower costs
Products Using VESA DSC

- Qualcomm Snapdragon 820
- NVIDIA Tegra X1
VESDA DSC in Consumer Electronics Applications
Use Case: Mobile and Tablet Applications

- Application processor
- DDIC (Display Driver IC) and touch panel controller
Use Case: In-Car Video Applications

- Application processor
- Infotainment display module
- Video cameras
- HDMI sources
- Ability to transport multiple video sources simultaneously
- Automotive serial interfaces and transport
Use Case: AR / VR Head-Mounted Display

- Video capture
- Application processor and GPU
- Micro-display driver IC
Use Case: 8K Digital TV

- TVs, STBs, and DVRs
- Multimedia SoC processor
- TCON (Timing Controller)
- Inside 8K TV
- Based on DSC 1.2a
Use Case: USB Type-C Laptop & Extended Display

- USB Type-C triple use
  - Peripheral
  - DisplayPort (Alt Mode)
  - Power delivery
- Shared bandwidth
  - Ex. Dual external monitors
    USB Type-C DP 1.4 transport
  - Storage
  - Networking
- DSC usage saves bandwidth for other external devices (storage, networking)

Image Source: Cadence
Use Case: USB Type-C Laptop & Extended Display

- Laptop with GPU
- Dual external monitors
- USB Type-C DisplayPort 1.4 transport
How to Integrate VESA DSC in Your Next Design
VESD DSC Encoder and Decoder IP
How Are Images Processed by VESA DSC?

DSC Image Slicing
1920x1080 image divided in 16 slices of 480x270 pixles

4 Vertical Slices
Use Case: Two Vertical Slices

- Example: 4K video 60 fps
- ASIC with pixel clock at 350 MHz
- Each slice = 350 Mpixels / sec
- Two vertical slices are needed
- Number of slices need to match between DSC Encoder and Decoder
WQHD Mobile Application

1440 x 2560 x 60 fps  7 Gbps
WQUXGA VR Mobile Application

AP
GPU
DPU

Hardent

De-Receiver Preambles

APB Registers

Prediction, ICH, Rate Control, DSU_VLC

Input Control

Sub-stream Multiplexer

Rate Buffer & Soft Slices Multiplexer

SDI Formatter Video / Command Modes

DSI Host Controller

2400 x 3860 x 90 fps  24 Gbps

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Conformance Test Guideline (CTG)
FPGA Prototyping
More Information

• VESA DSC white paper

• VESA DSC standard overview
  – www.vesa.org/vesa-standards

• VESA membership
  – www.vesa.org/join-vesamemberships

• A Quick Guide To VESA DSC
Live Demo of VESA DSC

• Visit Hardent in the exhibitor area to see a live 4K demo of VESA DSC!
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