MIPI High Speed Serial Technologies: Debug & Conformance Testing Challenges and Solutions

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Agenda

- MIPI D-PHY℠ Overview of signal characteristics
- Measurement/Probing Challenges
- MIPI C-PHY℠ Overview of signal characteristics
- MIPI C-PHY℠ Clock recovery & Switching Jitter
- Stress signal generation for Receiver Testing
- Q/A
MIPI D-PHY : Signal Characteristics Overview

• Detection of LP-HS transition and timing measurements on that transition

• Dynamic switching of terminations between LP and HS mode

• Measurements on clock and data lanes verify voltage and timing parameters, separate LP from HS bits

• D-PHY v2.0 onwards included eye diagram and jitter measurements

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Probing without losing signal fidelity

• High speed mode, Low power mode
  – High impedance to 50ohm bus
• Access to tight test locations
## Probe lead length effects

<table>
<thead>
<tr>
<th>Length of the lead</th>
<th>Rise time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Adapter with full length wire</td>
<td>227ps 46% Overshoot</td>
</tr>
<tr>
<td>Adapter with half length wire</td>
<td>126ps 48% Overshoot</td>
</tr>
<tr>
<td>Adapter with quarter length wire</td>
<td>59ps 43% Overshoot</td>
</tr>
<tr>
<td>Adapter with no wire</td>
<td>52ps 40% Overshoot</td>
</tr>
</tbody>
</table>

![Probe lead length effects](image-url)
Probe impedance

Differential Input Impedance (Ω)

Input Frequency (Hz)

100k 10k 1k 100 10k 100k 1M 10M 100M 1G 10G

High impedance
Lower impedance

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Measurement to be immune to instrument noise

- MIPI D-PHY: LP Slew rate measurement limit of 150 mV/ns
  - 50mV sliding vertical window, and average of all the edges
- A LPF filter to limit the high frequency noise

![Slew Rate Measurement Diagram](image)

Note that this slew rate measurement is very sensitive to high-frequency noise (contributed primarily by the DSO), which can translate to high-frequency deviations in the slew rate curve data. Because it is not desirable to include these deviations in the measurement, it is advantageous to filter the source waveform prior to performing the slew rate measurement, which will remove the high-frequency deviations. **To reduce the measurement noise, a 400-MHz, 4th-order Butterworth lowpass filter** will be applied to the source waveform prior to performing the measurement. (Note that for simplicity, the test filter will be used for all tests 1.1.x and 1.2.x, however the benefit
Debugging using Jitter extrapolation

- MIPI D-PHY Tx HS Eye Diagram
- Analysis of Continuous (Recommended) or Burst Data

- Analysis duration
  - (1) Sufficient to analysis at BER 1E-6 (Prorated Mask)
  - (2) Desirable to analysis at BER 1E-12
    - Sophisticated extrapolation software

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MIPI C-PHY: Signal Characteristics Overview

- 1st triggered edge recovered from A, B, and C wires
- Eye mask placement for optimal eye opening
- Rise/fall times are different for different transitions
- Derive three differential signal from 3 wire signal
- All the three eye diagram to be tested (VAB,VBC,VCA)
Switching Jitter and RT/FT

• Switching Jitter varies with number of Transition at the cross over.
• Data Jitter is 92psec, clock jitter is 61psec. Increment in clock jitter is not the same reflected in data, but increased by 3 folds (means 15 psec on clock increases data jitter by about 40 psec)
Switching Jitter based on Transition Type

<table>
<thead>
<tr>
<th>Transition Type</th>
<th>Min UI(ps)</th>
<th>MAX UI(ps)</th>
<th>Mean</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single</td>
<td>340.6</td>
<td>436.95</td>
<td>389.83</td>
</tr>
<tr>
<td>Double</td>
<td>368.4</td>
<td>469.4</td>
<td>409.9</td>
</tr>
<tr>
<td>Triple</td>
<td>359.27</td>
<td>457.1</td>
<td>401.6</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Transition Type</th>
<th>Min Time</th>
<th>Max time</th>
<th>Mean</th>
</tr>
</thead>
<tbody>
<tr>
<td>Double</td>
<td>20</td>
<td>71</td>
<td>45</td>
</tr>
<tr>
<td>Triple</td>
<td>0.97</td>
<td>61</td>
<td>29</td>
</tr>
</tbody>
</table>
Unit Interval Analysis of stressed signal

<table>
<thead>
<tr>
<th>Transition Type</th>
<th>Min(psec)</th>
<th>Max(psec)</th>
<th>Mean(psec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single</td>
<td>266.74</td>
<td>507.7</td>
<td>383.84</td>
</tr>
<tr>
<td>Double</td>
<td>323.23</td>
<td>559.83</td>
<td>418.29</td>
</tr>
<tr>
<td>Triple</td>
<td>302.4</td>
<td>508.41</td>
<td>393.99</td>
</tr>
</tbody>
</table>

Time difference of transition $\Delta t$

<table>
<thead>
<tr>
<th>Transition Type</th>
<th>Min(psec)</th>
<th>Max(psec)</th>
<th>Mean(psec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Double</td>
<td>55.95</td>
<td>178.48</td>
<td>111.9</td>
</tr>
<tr>
<td>Triple</td>
<td>5.193</td>
<td>158.2</td>
<td>55.6</td>
</tr>
</tbody>
</table>

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Switching Jitter with stress signal can affect the clock recovery

Clock Recovery works fine as long as unit interval variance due to switching jitter less than 0.5UI. If not, then clock recovery will lock the data either early or late arrival data and results in Mask violation. Clock transition is missed because of an ISI coupled with switching jitter.

How the clock is missed?

We assume that jitter is less than 0.5UI. The difference between early occurrence and late occurrence of the transition of the differential signal can be less than 0.5UI.
Receiver Testing

- **Philosophy**
  - Stimulus calibration based on parameter
  - Stimulus fed to the Rx
  - Check for error free reception

- **Equipment**
  - Waveform Generator
    - Data and clock lanes
  - Oscilloscope for Calibration
  - Choice based on MIPI D-PHY/C-PHY spec

- **Observables**
  - Bit errors detected
MIPI C-PHY Receiver Test: Signal Generation

- Monotonic signal generation
- C-PHY Encoding – bits, symbols, wire states
- Pseudo Random test patterns PRBS9/11/18

Stressors
- rise/fall time, duty cycle distortion (DCD), ISI,
- Differential and Common mode voltage control
- RX Test scenarios
  - Sequencing different waveforms created using LP, HS and LP-HS Mode
  - Defining various start up sequences by varying different parameters like jitter, length of sequences and looping these sequences
  - Fine granularity and control of various parameters like pre-amble, sync, post-amble
  - Ability to create waveforms for LP Only, HS only and LP-HS transition

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Rx test parameter precision, flexibility & range

- Clock Lane
  - Dp/Dn

- Disconnect Terminator

- Symbol: first

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- D-PHY

- C-PHY

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Multilevel Signal: Duty Cycle Distortion

- C-PHY receiver stress with Duty Cycle Distortion

- A symbol interval, all the lines would have the same DCD(Δ), but this would change with every symbol
Link Analysis

- Maximize Margins - Compensate for margin loss due to test fixtures
- Remove Reflections
- Open Closed Eyes - Apply receiver equalization to compensate for channel loss before analysis
- Compliance Test - require de-embedding, channel embedding, and equalization

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Backup
D-PHY Rx Jitter Tolerance

- RT/FT Control
- Insertion Loss
- De-Emphasis
- Periodic Jitter & VOD Control
- Static Skew
- DC common Mode
- SSC

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D-PHY Tx Test: Spread Spectrum clocking

- **SSC Testing**
  - Modulation Rate = 30KHz (min)
  - Measure over =>2 SSC cycles
  - Device Test Modes/options
    - HS data length > 66 μsec
    - HS data ‘101010...’