MIPI® A-PHYSM:
Laying the Groundwork for MIPI’s Automotive SerDes Solutions

MOBILE & BEYOND
Presentation Outline

MIPI A-PHY – System View
Ariel Lasry
Director, MIPI Alliance Board of Directors

MIPI A-PHY – Specification Overview
Edo Cohen
MIPI A-PHY Subgroup Vice-Lead

Q&A
MIPI A-PHY – System View
Ariel Lasry - MIPI Alliance Board Director
CASE:
- Connected
- Automated
- Shared
- Electrified

- Connected: The move to 5G
- Automated: The move to L2/L2+ and beyond
- Shared: New OEMs, new business models, new alliances
- Electrified: Tesla and others

And . . .

Safety: Improved government safety regulations (FCWS, AEB, RVS, LDWS, etc.)
Fuel economy: Aggressive regulations

Honda and GM Partner to Develop Mass Produced, Driverless Cars
Source: October 4, 2018, Automotive News

MIPI directly supports CASE via:
- Connected (MIPI RFFE\textsuperscript{SM}, others)
- Automated (MIPI A-PHY, MIPI CSI-2\textsuperscript{SM}, others)

RFFE: RF Front End
FCWS: Forward Collision Warning System
LDWS: Lane Departure Warning System
AEB: Autonomous Emergency Breaking
RVS: Rear View System

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NCAP Regulations Driving Sensors & Display Adoption

- Worldwide NCAP ADAS and ADS standards driving adoption of multiple high data rate “surround sensors”
- Displays for driver viewing of assistance imaging and information also require
What is MIPI A-PHY?

- MIPI A-PHY is a physical layer specification targeted for ADAS/ADS surround sensor applications and Infotainment display applications in automotive. Version 1.0 will provide a 15-meter reach and data rates of 2-16 Gbps, with a roadmap to 24, 48 Gbps and beyond.

- MIPI A-PHY is the ONLY standard interface to support native camera (MIPI CSI-2SM) and display (MIPI DSI-2SM) interfaces for automotive. An adaptation layer is also being developed for VESA DisplayPort and eDP.
Challenges to be solved require: A-PHY + MIPI Protocols

Robust Automotive Long Reach Link
- PER = $10^{-19}$: 1 packet error in ~10000 car-lifetimes
- High Speed Downlink and aggregation to support multiple 4K cameras and displays
- Asymmetric high speed link with fixed low latency ~6µs @G5

End to End Functional Safety
- Enabling Integration of devices using MIPI protocols over A-PHY in ASIL B or ASIL D Systems
- A-PHY and Protocols (CSI-2, DSI-2) FuSa from Source to Sink

End to End Security
- Authentication; prevention of tampering (malicious and non-malicious)
- High Definition Content Protection (HDCP) for display applications

Heterogeneous Interfaces
- Common support for multiple display protocols: DSI, Display Port, eDP, OpenLDI
- Agnostic to source/sink PHY configuration: C-PHY, D-PHY, Lanes count
MASS: MIPI Automotive SerDes Solutions

A vision for End-to-End System
Automotive Protocol Stack-up Diagram

Applications

MIPI Protocol Layers

Protocol Adaptation Layer (PAL)

Link Layer

Physical Layer

MIPI Camera / Radar / Lidar

MIPI CCS

MIPI Camera Service Extensions (CSE)

MIPI CSI-2

MIPI PAL/CSI-2

MIPI Display

MIPI DCS

MIPI Display Service Extensions (DSE)

MIPI DSI-2

MIPI PAL/DSI-2

Low Bandwidth Interfaces

Various Controllers

Future

GPIO

PC

I3C

VESA Display

VESA eDP/DP (SDP, MST, DP HDCP)

MIPI PAL/eDP-DP

MIPI PAL/eDP-DP for I2C/I3C/GPIO

MIPI A-PHY Data Link Layer

MIPI A-PHY SerDes — PHY Layer

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MIPI A-PHY – Specification overview
Edo Cohen - MIPI A-PHY Subgroup Vice-Lead
Gears and Profiles

- One Rate/line-code/modulation per Downlink Gear
- Single Uplink Gear
- Two Noise/Performance Profiles (with full inter-profile interoperability):
  - **Profile 1**: optimized for low cost/power implementations for the lower gears with lower Noise immunity and target PER of $<10^{-9}$
  - **Profile 2**: optimized for Vehicle Life-span, link robustness for all Gears with high noise immunity and target PER of $<10^{-19}$
- A-PHY Device supporting Gear N (N could be 1–5) shall support all lower gears.

<table>
<thead>
<tr>
<th>Gear Data Rate</th>
<th>Modulation [One modulation per Gear]</th>
<th>Symbol Rate [GBaud]</th>
<th>Net Application Data Rate [Gbps]</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>G1</strong> 2 Gbps</td>
<td>NRZ-8b/10b</td>
<td>2</td>
<td>1.5</td>
</tr>
<tr>
<td><strong>G2</strong> 4 Gbps</td>
<td>NRZ-8b/10b</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td><strong>G3</strong> 8 Gbps</td>
<td>PAM4</td>
<td>4</td>
<td>7.2</td>
</tr>
<tr>
<td><strong>G4</strong> 12 Gbps</td>
<td>PAM8</td>
<td>4</td>
<td>10.8</td>
</tr>
<tr>
<td><strong>G5</strong> 16 Gbps</td>
<td>PAM16</td>
<td>4</td>
<td>14.4</td>
</tr>
<tr>
<td><strong>Uplink, All Gears 100Mbps</strong></td>
<td>NRZ-8b/10b</td>
<td>0.1</td>
<td>0.055 (55Mbps)</td>
</tr>
</tbody>
</table>
Interconnect Channel

- A-PHY is a single lane, point-to-point, serial communication technology
- Support for multiple cable types – SDP/Coax
- Power over Cable support
- Up to 15m with 4 inline connectors
High Level Structure

• Native Protocol
  – e.g. MIPI CSI-2, MIPI DSI-2, I2C, GPIO

• Protocol Adaptation Layer (PAL)
  – Mapping to/from Native Protocol to A-Packet

• APPI
  – Interface between A-PHY Port and PAL

• Data Link Layer
  – Performs A-Packet scheduling, prioritization and forwarding

• Physical Layer
  – Encodes and decodes symbols extracted from A-Packets according to the modulation scheme used per Gear.
    – Modulated symbols are transmitted and received over the A-PHY interconnect according to the medium-dependent electrical specifications
PHY Layer

- Unified structure to reduce complexity
- Shared 8B/10B PCS for G1/G2 and Uplink
- RTS Sub-Layer
  - Manage Data Pacing and buffering
  - Assign Message Counter (MC) and CRC
  - P2 - the retransmission process for A-Packets that are erroneous or that are not received
- PCS Sub-Layer
  - specifies the conversion of Data Link Layer A-Packets into PHY Symbols.
  - In P2, PCS also handles the JITC(*) Re-Training
- PMD Sub-Layer
  - Defines the electrical specifications and the physical medium

(*) JITC – Just In Time Cancelers (Cancellers that are used only when needed as channel changes)
RTS - Time Bounded Local PHY Level Retransmission

- **Time Bounded**
  - Retransmission is attempted only within predefined “Overall Delay” (e.g. ~6μS @G5)
- **Local PHY Level**
  - Transparent to upper layers
  - Happens within a single A-PHY Hop
- **Dynamically Modulated**
  - Retransmitted packets has better error resistant data payload Sub-Constellation.
- **Highly Reliable**
  - PER (Packet Error Rate) < 10^{-19}
- **Highly Resilient**
  - Overcome Thousands symbols-long Error bursts
  - Multiple 10s of mVs, instantly attacking, NBI Peak.
- **Low Overhead**
  - Overall PHY + Link < 10% ➔ 90% Net Data rate
Data Link Layer

• The A-PHY Data Link Layer is a protocol agnostic layer that performs scheduling, prioritization and forwarding of A-Packets.

• Each Protocol Adaptation Layer has at least one APPI connection to the A-PHY Data Link Layer.

• A-PHY Data Link Layer may be connected to multiple Protocols Adaptation Layers using a single Local Function.

• The A-PHY Data Link Layer may have a single A-PHY Network Function connected to it, or multiple A-PHY Network Functions.

• The A-PHY Data Link Layer Enables A-Packet:
  – Forwarding
  – Prioritization
  – Duplication
  – Scheduling
Functional Safety

- A-PHY packets are end-to-end protected as recommended in ISO-26262:2018:
  - CRC-32 for each packet, providing a Hamming-Distance of more than 3.
  - Message Counter that is 8 bits wide.
  - Timeout monitoring is fulfilled by the Keep-Alive function.
- The above measures are necessary to argue a high diagnostic coverage for a communication bus, per Table D.6 in ISO 26262-5:2018
- All other functional safety features necessary in order to fulfil the required system-level safety goal with ASIL is expected to be managed by upper layers.
Noise Immunity

• There is a major variance in the OEM EMC requirements, from those who aim for minimal noise immunity, to OEMs that apply stringent requirement to protect their system.

• A-PHY two profiles provide two noise immunity levels, to accommodate this variance.
  – P1 has lower noise immunity, similar to other SERDES solutions and is applicable for G1 and G2 (optional G3).
  – P2 has very high noise immunity based on MIPI Alliance analysis of expected noise level for the car life-time period.

• MIPI conducted multiple tests in an independent labs evaluating the noise levels and shielding effect degradation after mechanical stress and aging.
  – The results helped evaluate the different available technologies.
  – The research continues as part of MIPI A-PHY SG activities.
Characteristics of RF Ingress Test

**Test Conditions**

**Cable:** Two types of Dynamics Coax cables in length of 2m and 15m

**Lab Conditions:**

- **Bending Fatigue & Temperature Cycling Test**

<table>
<thead>
<tr>
<th>Mechanical condition</th>
<th>Bending angle</th>
<th>180°</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bending diameter</td>
<td>60 mm</td>
<td></td>
</tr>
<tr>
<td>Bending Speed</td>
<td>10 times/min</td>
<td></td>
</tr>
<tr>
<td>Weight load</td>
<td>3 N (~0.3kgf)</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Temperature condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temp. cycle</td>
</tr>
<tr>
<td>Temp. range</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Total number of bending</th>
<th>36000 times</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total time</td>
<td>Roughly 72 hours</td>
</tr>
</tbody>
</table>

**Screening Attenuation Test Result**

![Graph of Screening Attenuation Test Result]

- **Dynamic Coax 1**
  - **After aging**
  - **ARD limit**
  - **Before aging**

- **Dynamic Coax 2**
  - **After aging**
  - **ARD limit**
  - **Before aging**

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A-PHY Future Outlook

• MIPI is working on the upcoming MIPI A-PHY V1.1 release
• This is an incremental version to the A-PHY V1.0
• Main A-PHY V1.1 features
  – **Up to 32Gbps** throughput using Dual Lane Downlink support over STQ cables
  – Double Rate Uplink (DRU) with 125Mbps Uplink effective throughput
  – PAM-4 support for lower gears – Better noise immunity with lower working frequency enabling usage of lower costs cables and connectors
• Additional Protocol Adaptation Layers – 100Mbps ETH and I2S
Concluding Thoughts

• In-vehicle architecture is rapidly evolving . . .

• Increased focus on surround sensor applications for ADAS / autonomous driving . . . Best served by dedicated high-speed asymmetric interfaces from sensors to ECU.

• Standardization important for economies of scale, lower cost & greater capabilities.

• The native MIPI protocols (CSI-2, DSI-2, I3C, others, available in billions of devices) with A-PHY deliver enormous benefit to the automotive industry . . . performance, cost, noise immunity, and long-term EBOM reduction via elimination of interface bridges.

• The MIPI solution is being developed to meet the broadest spectrum of automotive industry needs . . . with anticipated SOP as early as 2024.
MIPI® DEVCON
VIRTUAL EVENT

THANK YOU

MIPI ALLIANCE DEVELOPERS CONFERENCE
22-23 SEPTEMBER 2020

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