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High Speed MIPI CSI-2 Interface
Meeting Automotive ASIL-B
Agenda

- Automotive SOC Design
- Renesas SOC System Overview and Challenges
- MIPI IP Design for Automotive
Automotive SOC Design

• Sensor signal controller & receiver
  - Multi parallel high-speed/high-resolution AFE channels
  - High speed parallel data acquisition, pre-processing & buffering
  - MIPI CSI-2 I/F for data transfer with up to 2.5Gbps/lane
  - AEC-Q100 compliance
  - ISO26262 ASIL-B compliance using highly flexible diagnostic with respect to permanent and transient failures including failure detection and correction
    • Device configuration and control Interface
    • Data acquisition, processing and buffering
    • Built In Self-Test & System Test support
  - Sensor signal timing generation and control
  - Safe-SPI I/F for configurability and controllability
Automotive SOC Design

Autonomous vs Infotainment

• Safety critical application
  – Process compliance to AEC-Q100 + ISO26262
• Challenging Safety critical Failure In Time (FIT) requirement
  – Driving failure detection, diagnostic architecture (technology, circuit, etc.)
  – Failure prevention by material selection (e.g. Ultra Low Alpha (ULA) package components)

• Extended temperature range operation
  – Tjunc up to 150°C
• Integration of 3rd Party IPs supporting ISO26262 requirements
• Intensive thermal performance analysis & power optimization
• System level diagnostic support capability
Overview Of System Design

Renesas SOC

- **Actuator**
- **Actuator Supply**
- **Actuator Control & Signal Generation**
- **Timing & Data Acquisition Control**
- **Support Functions**
- **Host-IF**
- **FuSa Monitoring & Assessment**
- **MIPI CSI-2 D-PHY / 4 Lanes**

- **Multi-channel Sensor**
- **Multi-channel A2D Converter**
- **Parallel Data Acquisition**
  - **Pre-processing**
  - **Storage**
  - **MIPI-IF**

- **Sensor Supply**
- **Sensor Monitor**
- **Sensor Diagnostic**

- **Actuator Control & Signal Generation**
- **Timing & Data Acquisition Control**

- **Analog Functions**
- **Digital Functions**
- **Electronic Control Unit**

- **Module (Sensor)**
- **ECU**
Overview Of System Design

• Functional description & performance requirements
  – AEC-Q100 supporting Tj=150°C
  – ISO26262 ASIL-B supported by
    • Internal safety mechanisms for data path, configuration, supply monitoring, ...
    • External safety mechanisms for module level data path and supply monitoring
  – Actuator control and signal generation using GHz time base (supports cm level resolution)
  – Timing and data acquisition control operating at hundreds of MHz
Overview Of System Design

• Functional description & performance requirements (cont.)
  – Multi-channel sensor interface w/ parallel channel acquisition using
    • Ultra-low noise high BW sensor sensing amplifier
    • High speed 14-bit hundreds of MSPS A2D converter
  – Data acquisition pre-processing, storage and internal MIPI-Interface control
  – MIPI CSI-2 Data Interface for acquisition data transfer w/ 4 Lanes and up to 10Gbps to HOST-ECU
  – Safe-SPI Host-ECU Interface for configuration & failure handling
Unique Challenges To Renesas

• Very high transient failure rates
  – Driven by big amount of volatile memory (e.g. SRAM, DFF, etc.)
  – Error detection / correction using
  – ECC (SEC/DED) for internal data buffer
  – CRC for acquisition data to data buffer
  – MIPI CSI-2 data integrity (from buffer, Packet loss, footer w/ diagnostic information)

• Sensor signal timing generation and control accuracy (single digit GHz PLL / System base clock)
  – e.g. Single digit ps jitter rms
Unique Challenges To Renesas

- High speed / resolution parallel AFE control, data acquisition/pre-processing & buffering
- Many “firsts” for Renesas
  - First time use of 28nm technology
  - First time use of system in package / flip chip in BGA package
  - First time MIPI CSI-2 in automotive project
ISO 26262 Effort & Challenges

- Integration of 3rd Party IP’s supporting ISO26262 requirements
- IP provider preparing ISO26262 Safety Case
- Development and alignment on FuSa requirements and their adaption to the IP
- Development processes according to AEC-Q100, IATF 16949:2016 and ISO26262
- Soft Error Rate (SER), caused by high speed neutrons and alpha particles, is largely the dominating source of failure rate (> 20,000 FIT)
  - This required a concurrent set of very effective counter measures
ISO 26262 Effort & Challenges

• SER mitigating measures:
  – Replacement of standard mold compound (\(\sim 0.1 \alpha \cdot \text{cm}^{-2} \cdot \text{hr}^{-1}\)) and solder bumps (\(\sim 1 \div 10 \alpha \cdot \text{cm}^{-2} \cdot \text{hr}^{-1}\)) with Ultra Low Alpha (ULA) mold compound and bumps material (\(\leq 0.002 \alpha \cdot \text{cm}^{-2} \cdot \text{hr}^{-1}\)).
  – Generation of SRAM with a high level of columns and rows multiplexing (MUX \(\geq 8\)). This prevents SER to generate Multiple Bit Upset (MBU) within the same word line.

• SER detecting measures:
  – Instantiation of 1-bit error correction (ECC) and 2-bit error detection (EDC) encoder/decoders for each memory
  – Checksum
• SEC/DED safety mechanism alone is partially effective
• However, with the above example, with BL > 2, error detection is not ensured
The SBU Solution

- Memory cells belonging to the same data word are distributed to each other far away.
- Thus, every SER event resulting in MCU > 0 is converted into a correspondent number of SBUs that can be individually detected and corrected.

SEC-DEC safety mechanisms does not correct dual errors

SEC-DEC safety mechanisms does detect and correct single-error
Auto vs Standard MIPI IPs

- Reliability
- Safety
- Testability
- Performance
Reliability

Reliability can be opposite to Safety!

- AEC Q100 ambient Temperature
  - Grade 1: 125°C → 150°C junction temperature
- Mission Profile of the environmental stressor
  - Caused by EM and Aging effects.
- Design Margins and CPK
  - For QM: CPK = 1
  - For ASIL: CPK = 1 → 2
- Extended PVT sign-off corners
- Aging Simulations and Self Heating
Safety: SEooC and AoU

- IP vendor has no prior knowledge of system
- Assumptions on Safety Functions
- AoU
  - Target ASIL
  - Operating Conditions for PHY
  - BIST Modes
  - Input Clock frequency requirements
  - Temperature Mission Profile
  - Sources of Baseline Failure Rate
    - e.g. Siemens SN 29500, IEC 61709, etc.
    - Transient Failures from high speed neutrons and alpha particles
Safety: DFMEA

- Dependent Failures: Internal and External
- Each failure effect
  - Assigned severity rating
  - Correlated with the risk associated
- Ensure coverage of all systematic faults
- Outputs:
  - Identification and execution of Corrective Actions
  - DFMEA database and report
  - Qualitative analysis is key for quantitative analysis
  - Failure modes re-use in FMEDA
Safety: FMEDA

- Hardware Safety Requirements
  - PLL to generate healthy clock
  - HS bursts must be transmitted correctly
- BFR for PRF set based on IEC 61709

Safety Mechanisms
- Internal
- External
  - MIPI D-PHY RX
  - MIPI CSI-2 RX
  - SOC RX
- FIT linked to the technology / package / temp
Safety: Safety Manual

- AoU
- Assumed Hardware Safety Requirements
- Safety Goal Violations
- Safety mechanisms
  - Internal and External
- Safety analysis
  - DFMEA, FMEDA, DFA
- Safety Lifecycle Tailoring for IP
Testability

- **IP Configurations**: MIPI C-PHY, MIPI D-PHY, and MIPI C-PHY/MIPI D-PHY
  - Universal
  - MIPI CSI-2 TX+ / MIPI CSI-2 RX+
  - MIPI DSI TX+ / MIPI DSI RX+
- **Loopback BIST**
  - LB BIST enables periodic checking of faults
  - Helps achieve higher ASIL grade
- **Lab validation**
  - Using Loopback BIST
  - Eye-Diagram and compliance test
  - BER profiling for QoS assessment
- **ATE validation**
  - Using Loopback BIST
  - Full temperature range coverage by execution at 3 corner temperatures
Performance

- High bandwidth to allow higher sensor resolution and higher dynamic range
  - Up to 30Gbps in MIPI C-PHY/MIPI D-PHY
  - 4.5 Gsps IP

- Area

- Low EMI

- Risk Mitigation
  - Integrated MIPI sub-system
  - Deep MIPI system and SerDes expertise
Auto Grade IPs

- World-class knowledge of MIPI IP
- Integrating MIPI subsystems into your SOC, safely
- Providing on-chip safety mechanisms to achieve higher system ASILs
- Widest errors detection coverage (> 98%)

- IP Auto grades: ASIL B & D
- Temperature Grade: 1 & 2
- Minimum CPK: 1-2
- Functional Safety Packages
  - Level 1 – DFMEA
  - Level 2 – FMEDA and Safety Manual (ASIL Ready)
  - Level 3 – Full ISO 26262 Functional Safety certification
### ADDITIONAL RESOURCES: GLOSSARY

- AEC – Automotive Electronic Council
- AFE – Analog Front End
- AoU – Assumptions of Use
- ATE – Automatic Test Equipment
- ASIL – Automotive Safety Integrity level
- BFR – Baseline Failure Rate
- BIST – Built In Self Test
- BW – Bandwidth
- CRC – Cyclic Redundant Check
- Cpk – Process Capacitance index
- DED – Dual Error Detection
- DFA – Dependent Failure Analysis
- DFMEA – Design FMEA
- ECC – Error Correction Code
- ECU – Electric Controller Unit
- EMI – Electro-Magnetic Interference
- FMEA - Failure Mode and Effect Analysis
- FIT – Failure In Time (i.e. per Billion of hours)
- FMEDA – Failure Mode and Effect Analysis with Diagnosis
- IP – Intellectual Property
- MBU – Multiple Bit Upset
- MCU – Multi Cell Upset
- PHY – PHYsical hardware layer
- PLL – Phase Lock Loop
- PRF – Permanent Random Failures
- PVT – Process, Voltage Temperature corners
- QM – Quality Management (e.g. IATF 16949, ISO 9001, etc.)
- SBU – Single Bit Upset
- SEC – Single error Correction
- SER – Soft Error Rate
- SPI – Serial Parallel Interface
- SOC – System On Chip
- SRAM – Static Random-Access Memory
- ULA – Ultra Low Alpha
Mipi DEVCON
VIRTUAL EVENT

THANK YOU

Mipi Alliance Developers Conference
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