Geoffrey Duerden
Introspect Technology

Interoperability Challenges and Solutions for MIPI I3C℠
Interoperability Challenges and Solutions for MIPI I3C℠

• I3C: A Brief Overview
• Interoperability Challenges
  – Board layout and component optimization
  – Signal timing adjustment
  – Protocol implementation
• Conclusions and Best Practices
To begin... what is MIPI I3C℠?

- What makes I3C so innovative?
  - I3C introduces higher bandwidth operating modes
  - I3C provides a very flexible system architecture
  - I3C has the potential to reduce pin counts on sensor interfaces
MIPI I3C℠ Data Rates

- Open Drain: up to 4.0 MHz
- Push Pull: up to 12.5 MHz
- HDR-DDR: up to 25 MHz
- HDR-Ternary: up to 33 MHz
- MIPI I3C v1.1 has new modes as well

Open Drain Waveform

Push-Pull Waveform
MIPI I3C℠: Interoperation

- The vision for the I3C is that it will be adopted within multiple sensor and controller applications.
- I3C implemented by different manufacturers and industries, often with very different control and bandwidth requirements.
- Legacy I2C devices can be placed on the bus too.
Board Design and Layout

• Some basic guidelines: attention to power and ground
  – On left: master and slave on separate ground planes, connected by wire
  – On right: master and slave on the same ground plane
Board Design and Layout

• Some basic guidelines: design boards with testing in mind
  – On left: 3 x 6 inch traces for 3 x I2C devices connected to bus
  – On right: with jumper removed, the 3 x 6 inch traces are removed from bus

Reflection near mid-voltage level
Open Drain and Component Optimization

• Can you interoperate with a very capacitive bus?
  – Typically, use $R = 2.83 \text{k}\Omega$ for pull up resistors
  – This assumes rise time = 120 ns, line capacitance = 50 pF

• Problem: what if bus capacitance is as high as 180 pF!
• In this case, can only interoperate up to a data rate of 1.2 MHz

SCL = 1.2 MHz
Open Drain and Component Optimization

• Problem: how can the RC time constant be reduced to allow 4 MHz open drain operation?
• Solution: reduce the pull up resistance.
• Trade off: must keep $V_{OD} < 270$ mV. The design meets $V_{OD}$ spec.

• Note reflection on SDA from 24 inch trace, with no back termination. There is time for the reflection to settle.
Push-Pull and Timing Control

- On left, successful interoperation at 10 MHz push-pull
- On right, interoperation failures at 12.5 MHz push pull
- Problem: SCL/SDA skew as a function of data rate
- One solution: adjust the sampling control on the master
More on Timing Control

- On left: open drain = 3.5 MHz operation
- On right: open drain = 4.0 MHz operation
- Look at acknowledge bit. With this DUT, acknowledge was not instantaneous
- Result: Slave doesn’t respond in time at 4.0 MHz
More on Timing Control

- One solution: master could delay the SCL edge during the acknowledge bit to provide additional time for slave to respond.

Extend the acknowledge bit timing
Protocol Implementation

• Interoperation example: Hot Join
Interoperation example: Hot Join

- After the slave's HJ request has been acknowledged, bus goes idle.
- This is an interoperation error.
 Protocol Implementation

- Interoperation example: Hot Join

- On left: after the slave's HJ request has been acknowledged, bus goes idle.
- On right: after the slave's HJ request has been acknowledged, the master issues a repeated start
Interoperation example: Hot Join

- On left: after the slave's HJ request has been acknowledged, bus goes idle.
- On right: after the slave's HJ request has been acknowledged, the master issues a repeated start.
Protocol Implementation

• Interoperation example: HDR-DDR
Protocol Implementation

- Interoperability example: HDR-DDR
  - Unsuccessful DDR write: the slave issues a NACK
  - Underlying issue: master is I3C version 1.1, slave is I3C version 1.0.
Protocol Implementation

- Interoperation example: HDR-DDR
  - On left: unsuccessful DDR write: the slave issues a NACK
  - On right: successful DDR write: the master receives an ACK from slave
Protocol Implementation

- Interoperation example: HDR-DDR
  - On left: unsuccessful DDR write: the slave issues a NACK
  - On right: successful DDR write: the master receives an ACK from slave
Protocol Implementation

- Interoperation example: HDR-DDR
  - On left: unsuccessful DDR write: the slave issues a NACK
  - On right: successful DDR write: the master receives an ACK from slave
  - Analyzer tools ensure interoperation debug goes smoothly
Conclusions and Best Practices

• MIPI® I3C℠ has great potential to provide a fast sensor and control bus, and can save a lot of pins on devices and traces on PCBs

• To help ensure interoperability:
  – First principles for layout
    • Power and ground, designing buses for test, bus capacitance
    • Understand signal timing issues
    • Small adjustments can make a big difference for interoperability
  – Protocol implementation
    • Having analysis tools can help make interoperability debug smooth
ADDITIONAL RESOURCES

- [https://www.mipi.org/specifications/i3c-sensor-specification](https://www.mipi.org/specifications/i3c-sensor-specification)  
  - MIPI® I3C℠ Specifications

- [https://www.mipi.org/sites/default/files/mipi_I3C-and-I3C-Basic_app-note-system-integrator](https://www.mipi.org/sites/default/files/mipi_I3C-and-I3C-Basic_app-note-system-integrator)  
  - System Integrators Application Note for MIPI® I3C℠ v1.0 and I3C℠ Basic v1.0

- [https://introspect.ca/](https://introspect.ca/)  
  - Total solutions for most high-speed interface technologies

- [https://introspect.ca/products-solutions/i3c-design-and-test/](https://introspect.ca/products-solutions/i3c-design-and-test/)  
  - I3C design and test solutions

- [https://register.gotowebinar.com/register/8766219688391017985](https://register.gotowebinar.com/register/8766219688391017985)  
  - I3C Webinar
Thank you