MIPI Alliance Display Webinar:

Display Developer Trade-offs When Using DSI with Compression, Segmented Panel Designs and Pixel Overlap between Segments

Dale Stolitzka
Samsung Display America Lab

Jeffrey Small
Synaptics, Inc
MIPI Alliance: A Brief Introduction

Peter B. Lefkin
Managing Director
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About MIPI Alliance

• 267 Members (as of 19 March 2015)
• 45+ specifications and supporting docs
• We drive mobile and mobile-influenced interface technology through the development of hardware and software specifications
• We work globally and collaboratively with other standards bodies to benefit the mobile ecosystem
MIPI Alliance Member Ecosystem

- Device OEMs
- Handset Manufacturers
- IP and VIP Providers
- Test Labs
- Test Equipment Companies
- Semiconductor Companies
- Software Providers
- Application Processor Developers
- Consumer Electronics – Camera, Tablet, PC/Laptop, Peripherals
Active MIPI Alliance Working Groups

- Analog Control Interface
- Battery Interface
- Camera
- Debug
- **Display**
- Low Latency Interface
- Low Speed Multipoint Link (New - SoundWire℠)
- Marketing
- PHY (C / D / M)
- Reduced Input Output (RIO) (New)
- RF Front-End (RFFE℠)
- Sensor / I3C℠ (New)
- Software (New)
- Technical Steering Group
- Test
- UniPro℠
MIPI System Diagram

* The UFS (Universal Flash Storage) specification from JEDEC, the SSIC (SuperSpeed Inter Chip) specification from USB-IF, and the M-PHY (Mobile PHY Express) specification from PCI-SIG all use the MIPI® M-PHY™ mark.

* UFS (Universal Flash Storage) specification is available from JEDEC and uses the MIPI® UniPort™. UniPort and M-PHY are registered marks and StrongMotion™ and SoundMotion™ are service marks of MIPI Alliance, Inc.
Recent Announcements

18 February 2015 - MIPI Alliance Updates its Widely Adopted CSI Specification to Bring High-Resolution Imaging, Richer Color and Video to Mobile and Mobile-Influenced Applications

12 March 2015 - MIPI Alliance Updates its MIPI RFFE Interface for Mobile Device RF Front-End Architectures
The Future of MIPI – Beyond Mobile

• Mobile influences **everything**

• Everything gets faster, smaller and lower power
  - MIPI will continue to evolve specs to take advantage of the evolution of technology in mobile devices
Visually Lossless Compression and Practical Tradeoffs for Developers

Dale Stolitzka
Samsung Display America Lab

25 March 2015
Discussion

• Problem Statement
• Compression for display streams
• Visually lossless quality testing
• Conclusions
Mind the gap

Display resolution CAGR >2x / year

PHY trend +20%/year

MPixels

PHY per Lane Gb/s

0.0

1.0

2.0

3.0

4.0

2011 WXGA

2012 HD

2013 FHD

2014 QHD

Samsung Galaxy S® II

Samsung Galaxy S® III

Samsung Galaxy S® 4 / 5

Samsung Galaxy Note® 4

Model data from Samsung Electronics, Co., Ltd. www.samsung.com/us/
Memory Compression Power and Area Tradeoff – UHD Example

\[ \text{Area}_{\text{Decoder}} < \text{Area}_{\text{RAM}} - \left( \frac{\text{compressed bit rate}}{\text{uncompressed bit rate}} \right) \times \text{Area}_{\text{RAM}} \]
Display stream signal chain

Pixel data → PHY → Bit Coding (if applicable) → Image coding → Link payload

- T: 1x
- T + 2 yrs: 1.44x
- 1x
- 1.23x
- 1x
- 2x~3x
- 3.4~5x

e.g. 8b/10b → 128b/132b
Compression Level

Compressed bit rate (bpp) = \[
\frac{\text{Link rate \( \frac{\text{bits}}{\text{sec}} \)}}{\text{Pixel rate \( \frac{\text{pixels}}{\text{sec}} \)}}
\]

• DSI supports three profiles:
  – Profile 12 = 12 bpp
  – Profile 8 = 8 bpp
  – Generic profile ≥ 8 bpp

• **Verify support** of profile(s) from the IC vendors
### MIPI DSI Compressed Interface

<table>
<thead>
<tr>
<th>Rows x Columns</th>
<th>Pixel rate (MP/s)*</th>
<th>Example Rates</th>
<th>Compression (bpp) †</th>
</tr>
</thead>
<tbody>
<tr>
<td>1600 x 2560</td>
<td>270</td>
<td>1 x 3 @ 1.1 Gb/s</td>
<td>12</td>
</tr>
<tr>
<td>2880 x 1800</td>
<td>350</td>
<td>2 x 1 @ 1.4 Gb/s‡</td>
<td>8</td>
</tr>
<tr>
<td>2160 x 3840</td>
<td>540</td>
<td>1 x 3 @ 1.5 Gb/s</td>
<td>8</td>
</tr>
<tr>
<td>3840 x 2400</td>
<td>620</td>
<td>2 x 2 @ 1.3 Gb/s‡</td>
<td>8</td>
</tr>
</tbody>
</table>

* Non-CVT pixel rates approximated for typical mobile display panels.
†: compression bit rate = floor (Link rate / Pixel rate)
‡: Examples of two panels using multiple DSI Links or a Multi-DSI Link.
Memory Compression in Olden Days

[Diagram showing the process of memory compression from an Application Processor to a Display Module]
DSI Link Compression Today

Application Processor with DSC 1.1

Encoder

Pixel Data

On-Chip Memory

(No Decoder)

TX Port

DSI 1.2 Interface

RX Port

Display Module with DSC 1.1

Decoder

On-Chip Memory

(No Encoder)

To Display
A Display Stream Coding Imperative

Invisible in both picture quality and latency
Noise and Mid-grey at 6 bpp

Excellent image photography codecs are not necessarily the right answer.
Subjective testing evaluates image quality

ISO/IEC IS 29170-2 test method

Which is uncompressed?
Objective metrics do not predict performance

Visually lossless
Barely perceptible
Impaired

\[ \log_{10}(\text{HDR VDP2}) \]

PSNR

Mean response fraction

Log \( \text{HDRvdp2} \)

Mean response fraction

PSNR

PSNR = peak signal to noise ratio
HDR VDP2 = high dynamic range visual difference predictor #2
## Subjective testing guidelines

<table>
<thead>
<tr>
<th>Display conditions</th>
<th>ISO/IEC IS 29170-2</th>
<th>ISO/IEC IS 29170-2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ISO 3664, ISO 9241-303</td>
<td>Image viewing</td>
</tr>
<tr>
<td>Monitor</td>
<td>Calibrated monitor</td>
<td>Image sets</td>
</tr>
<tr>
<td>Color</td>
<td>sRGB, BT.709, BT.2010</td>
<td>Video sets</td>
</tr>
<tr>
<td>Viewing distance</td>
<td>Distance at 30 PPD</td>
<td>SVT Fairytale and game screen captures</td>
</tr>
</tbody>
</table>

\[ E = 60 \text{ pixels/degree (PPD)} \]
Conclusions

• Hi-res display system design trade-offs
  – Bandwidth
  – IC area for memory
  – Power

• DSC 1.1 fulfills major industry needs

• Use subjective testing for image quality evaluation

• MIPI DSI fulfills all requirements and is available
Using Compression with Multiple DDICs

Jeffrey Small
Synaptics, Inc.

25 March 2015
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Multi-DDIC Topologies: TCON + Multiple DDICs

- One (or multiple) DSI link(s) to TCON
Multi-DDIC Topologies:
DSI Direct to Multiple DDICs

- Multiple DSI links, one to each DDIC
  - Or use a split DSI link
- One DDIC must be designated as the master
  - Remaining DDICs must be synched to the master DDIC
# Data Rates for “4K” Panel
(3840 x 2160, 60fps, 10% blanking, portrait mode, unmuxed RGB, 3:1 compression)

## TCON

<table>
<thead>
<tr>
<th></th>
<th>DPHY v1.1 (1.5Gbps/lane)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Total peak bit rate</td>
</tr>
<tr>
<td>No Compression</td>
<td>13.271Gbps</td>
</tr>
<tr>
<td>3:1 Compression</td>
<td>4.424Gbps</td>
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</table>

## No TCON → 3 DDICs

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# Data Rates for “4K” Panel

(3840 x 2160, 60fps, 10% blanking, portrait mode, unmuxed RGB, 3:1 compression)

<table>
<thead>
<tr>
<th>TCON</th>
<th>DPHY v1.2 (2.5Gbps/lane)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Total peak bit rate</td>
</tr>
<tr>
<td>No Compression</td>
<td>13.271Gbps</td>
</tr>
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<td>3:1 Compression</td>
<td>4.424Gbps</td>
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</tbody>
</table>

| No TCON → 3 DDICs     |                         |                     |             |           |             |
|                       | Total peak bit rate      | Bit Rate per lane   | # DSI Links/DDIC | Lanes/DSI | # Wires/DDIC  |
|                       |                           |                     |                             |             | (Total # Wires) |
| No Compression        | 13.271Gbps               | 2.212Gbps           | 1                           | 2           | 6 (18)       |
| 3:1 Compression       | 4.424Gbps                | 1.475Gbps           | 1                           | 1           | 4 (12)       |
Data Rates for “8K” Panel
(7680 x 4320, 60fps, 10% blanking, portrait mode, unmuxed RGB, 3:1 compression)

<table>
<thead>
<tr>
<th>TCON</th>
<th>DPHY v1.2 (2.5Gbps/lane)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Total peak bit rate</td>
</tr>
<tr>
<td>No Compression</td>
<td>53.084Gbps</td>
</tr>
<tr>
<td>3:1 Compression</td>
<td>17.695Gbps</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>No TCON → 6 DDICs</th>
<th>DPHY v1.2 (2.5Gbps/lane)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Total peak bit rate</td>
</tr>
<tr>
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DSI Data Synchronization

• Master DDIC generates glass timing
• In video mode, the remaining DDICs must be synched to the master’s horizontal blanking periods
  – Synchronization method is out of scope for DSI
  – However, DSI data corresponding to one line must be synched within the horizontal blanking period across all DSI links
• In command mode, data need only be synchronized across all DDICs relative to the TE signal
DCS Command Synchronization

- Each DDIC saves DCS commands in an internal queue
- The same commands should be sent to each DDIC
- Host sends the DCS “Execute Queue” command to the master when it is desired to execute the queued commands in each DDIC
- At the beginning of the next vertical blanking interval after receiving an Execute Queue command, the master DDIC executes its queued commands and signals the slave DDICs to do the same
Compression for Multi-DDIC Systems

• The compressed data for each DDIC must be completely independent of the data sent to the other DDICs
  – A given DDIC has no access to compressed data nor to decompressed data from the other DDICs

• For lossy compression, care must be taken to avoid visible seams at the image partition boundaries corresponding to each DDIC
Compression for Multi-DDIC Systems

- Avoiding visible seams requires the image to be partitioned into overlapping sections, where each section is independently compressed and sent to its corresponding DDIC
  - After decompression, the overlapping pixels are discarded by each DDIC
  - Even so, care must be taken when managing the compressors’ bit budgets so as to avoid lossy compression near the section boundaries

- There may be additional reasons to overlap the image sections
  - Image enhancement filtering in the DDICs
  - Certain panel architectures
Description of Overlapping Sections

- Define the coordinate system for each DDIC identically, with the origin in the upper left corner
  - The host must translate image coordinates to the corresponding coordinates for each DDIC’s image section
Compressor State Resetting for Multiple DDICs

- Many compressors partition the image into independent sections
- For each section, the compressor maintains a state that is a function of the previously compressed pixels for that section
  - E.g. VESA DSC v1.1 maintains an Index Color History (ICH) buffer for each section (slice)
  - When an image is compressed in raster order, the raster may cross more than one section
Rules for Resetting the Compressor’s State

- Every time that the compressor will cross the boundary between two slices, its state must be reset.
- Similarly, if the decompressor will cross the boundary between two slices, the compressor state must also have been reset.

Thus, when either the compressor crosses or the decompressor will cross the boundary between two slices, the compressor state must be reset.
Rules for Resetting the Compressor State

This may be stated as two rules (assuming compression of raster-ordered image data):

1. When the slice width is equal to the image width, the compressor state should be reset only once, at the beginning of the slice

2. When the slice width is not equal to the image width, the compressor state should be reset at the beginning of each line of each slice

The compressor state includes line buffers, pixel history, statistics, values that are used to adjust the instantaneous bit-rate, etc.
Resetting the Compressor State with Multiple DDICs

The portion of an image corresponding to one compressor or of one decompressor is defined as a “pane”. Each pane must be compressed independently. The two rules just described should thus be restated as:

1. When the slice width is equal to the pane width, the compressor state should be reset only once, at the beginning of the slice

2. When the slice width is not equal to the pane width, the compressor state should be reset at the beginning of each line of each slice

When the compressor pane width and decompressor pane width are unequal, one must use the smaller of the two pane widths when applying the above rules
Example Multi-DDIC Topology, showing “panes” and “slices”

1. Each decompressor is one slice wide
2. Each compressor is two slices wide, thus slice width ≠ pane width
3. The state must be reset at the beginning of each line of each slice, due to (2) above
Summary

• Using 3:1 compression, dual DSI links (4 lanes each) are sufficient to drive the TCON in an “8K” display

• With no TCON, because each DDIC drives only a portion of the image, one DSI link per DDIC is sufficient

• The DDICs must be synchronized to each other within one Horizontal blanking period

• DCS commands must be synchronized within one Vertical blanking period

• Adjacent “overlap” pixels must be appended to each DDIC’s data before compression

• The state of the compressor must be reset whenever it crosses a boundary or whenever the decompressor will cross a boundary
Thank You