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mipi alliance

# New Low Latency Interface Specification Eliminates Memory Chip

February 29, 2012

mipi alliance

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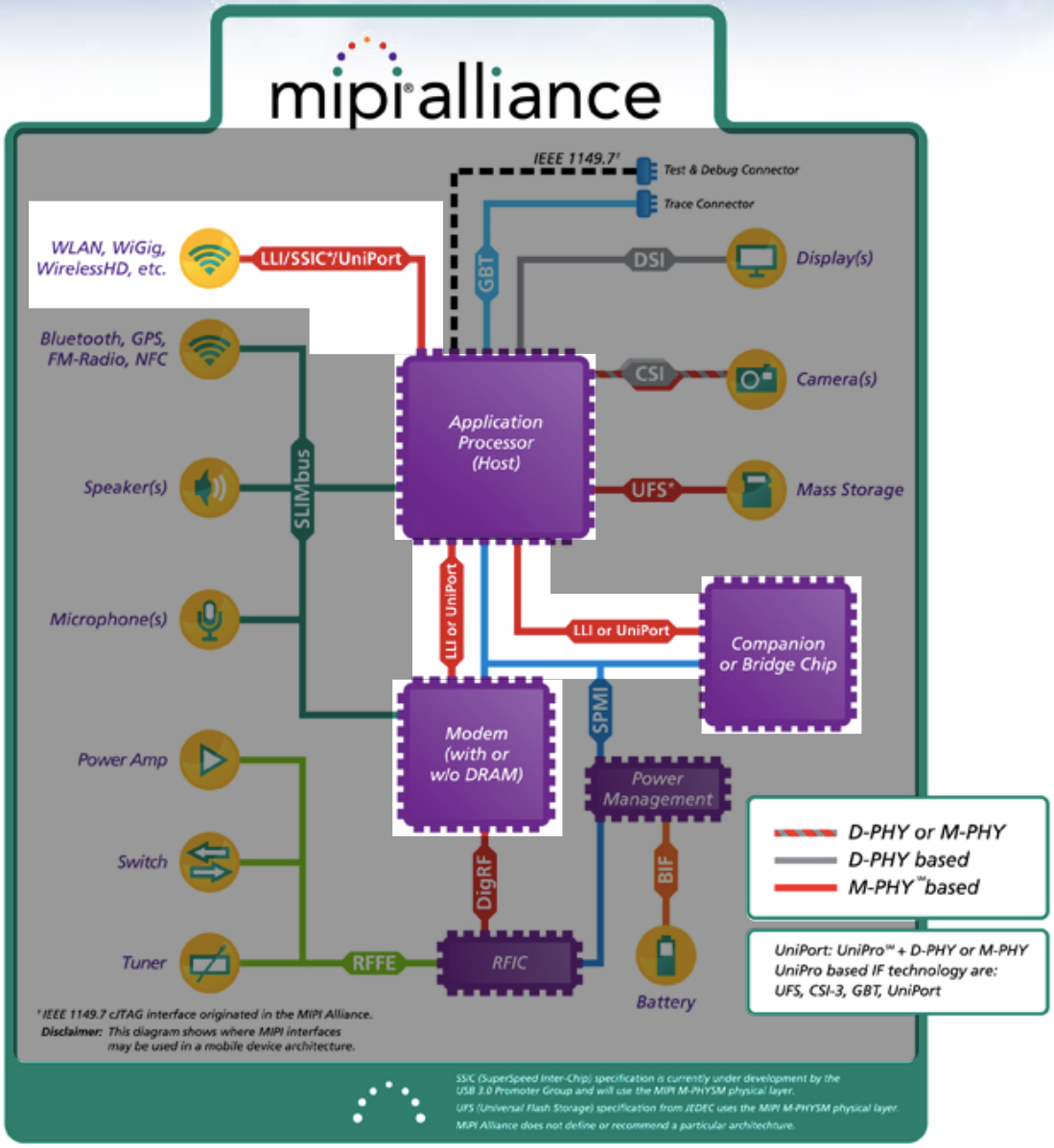
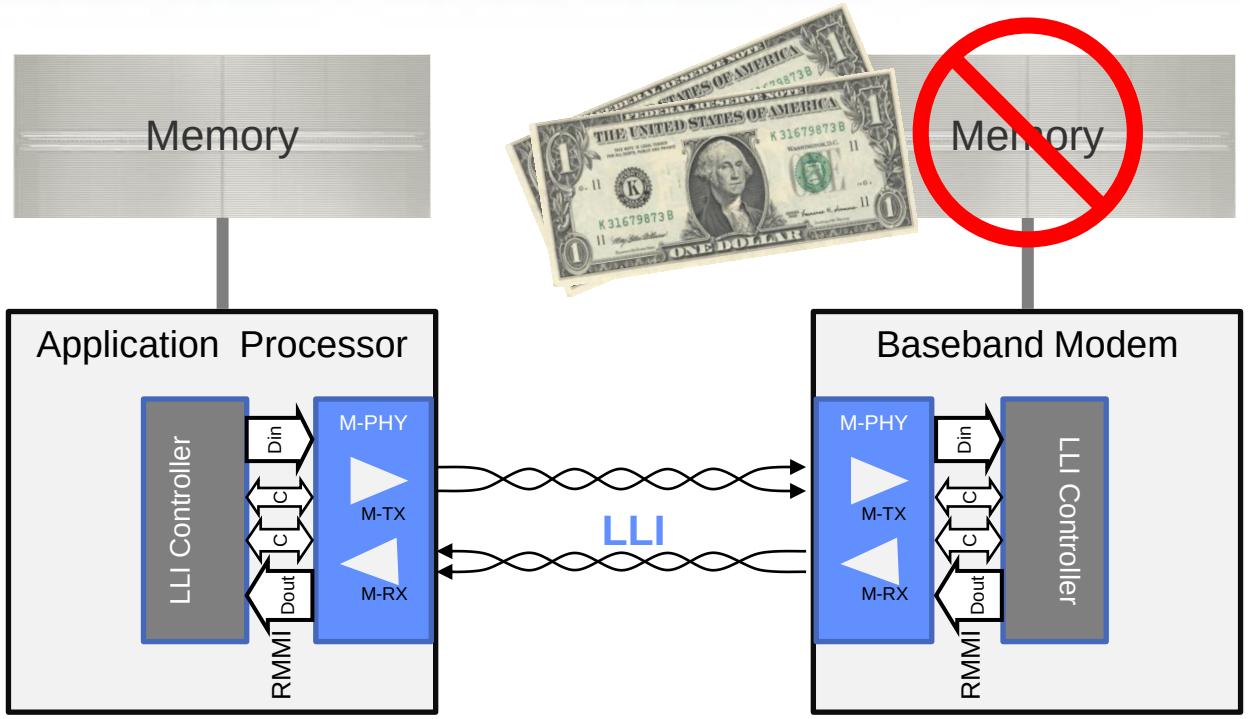


# What is MIPI LLI?

## LLI = **Low Latency** Interface

- Enables companion chip use models
- Fast enough for cache refills & DRAM sharing
- No software drivers or stack
- Minimal Pins
- Uses low power MIPI M-PHY

# MIPI LLI enables Shared Memory and Companion Chip use cases



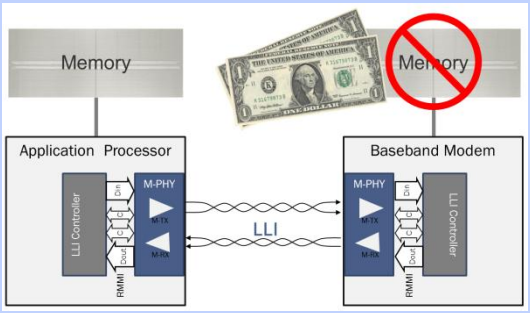

Removing an LPDDR2 saves $1-2

# MIPI LLI is less expensive than PoP

## Low Latency Interface

Removing modem baseband's dedicated memory:

- Saves $1-2 in BoM cost
- Eliminates DRAM area from PCB floorplan
- Maintains vertical height clearance




## Modem BB + DRAM PoP

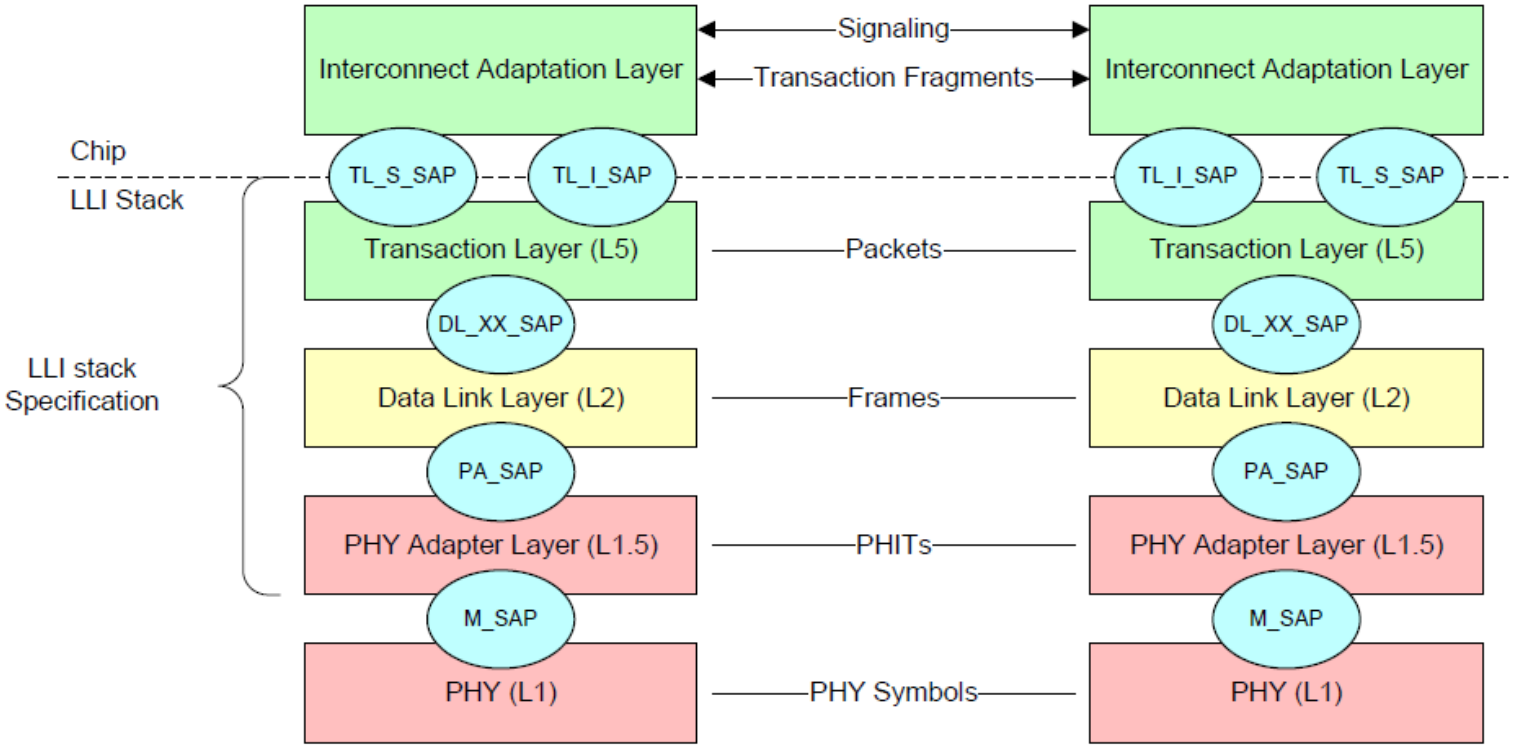
Using a modem baseband + RAM in a PoP:

- Maintains $1-2 RAM BoM cost
- Adds $0.50 to $1+ for PoP packaging cost
- Increases chip vertical height

# How Did We Get Here?

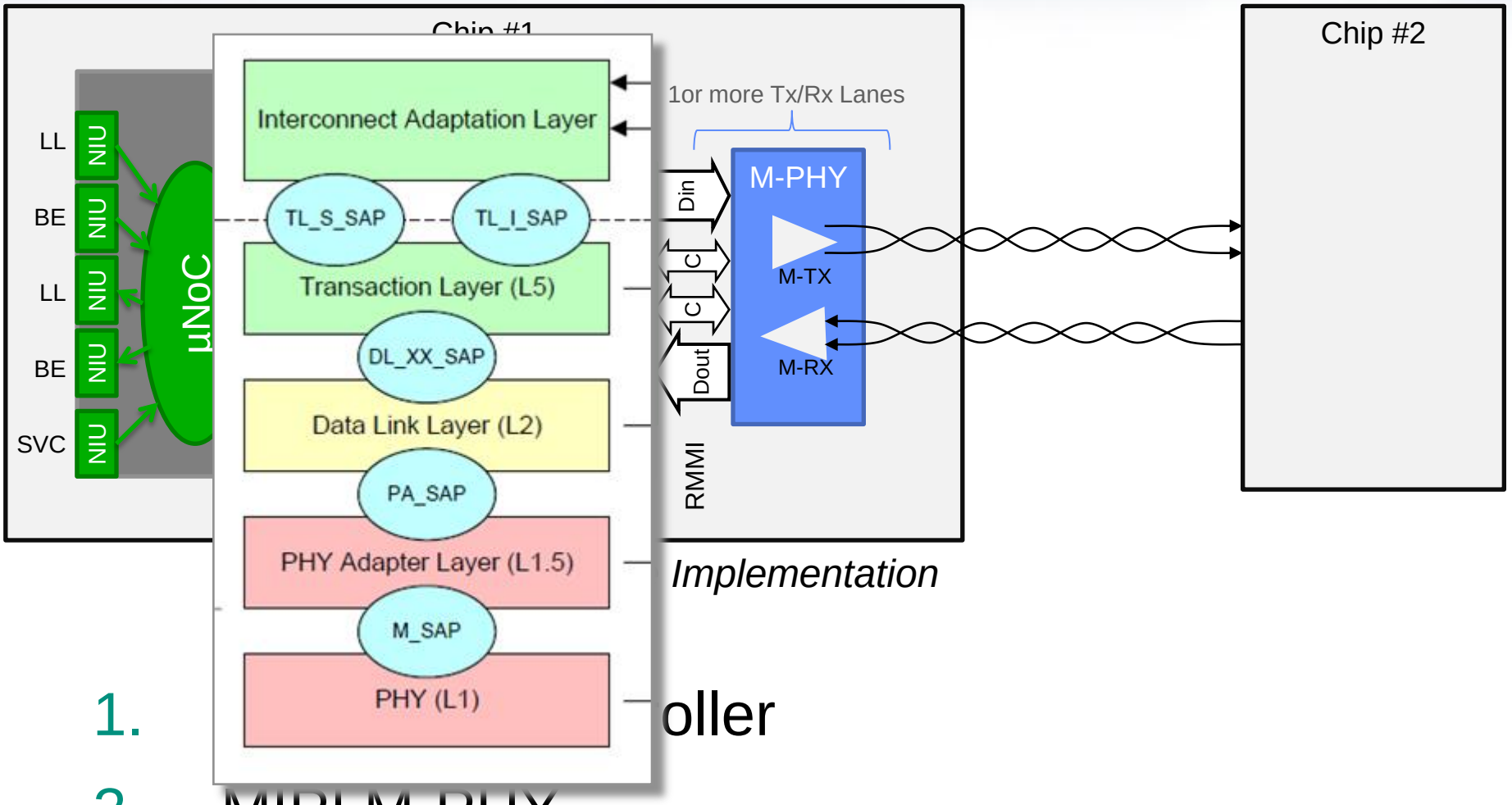
- LLI Investigation group formed in Dec 2009
- LLI confirmed as Working Group in March 18, 2010
- MIPI LLI 0.8 spec published Dec 16, 2010, voted August 2011
- MIPI LLI 1.0 spec approval target Q1 2012
- LLI WG Member Companies:
  - Analog Devices, ARM, Arteris, Broadcom, Cadence, Infineon, MCCI, Micron, Motorola, Nokia, Qualcomm, RIM, Samsung, SMSC, STMicroelectronics, ST-Ericsson, Texas Instruments

# LLI is a Layered Model




1. LLI Digital Controller
2. MIPI M-PHY

# LLI is Implemented in 2 Parts

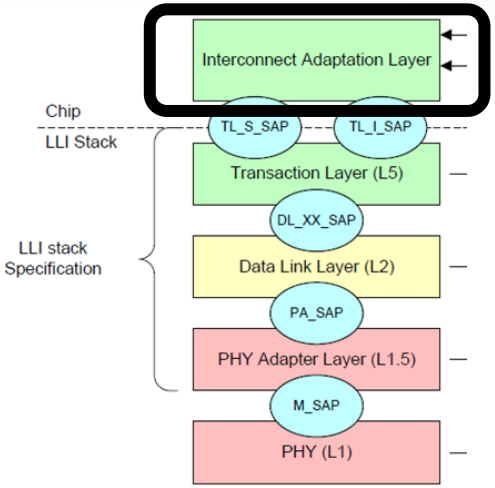


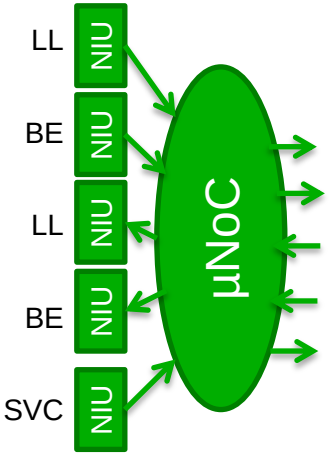

*Implementation*

1. oller
2. MIPI M-PHY

# Interconnect Adaptation Layer

- IAL is example implementation from Arteris
- Connects to SoC interconnect
  - Typically AXI, OCP for Low Latency (LL) and Best Effort (BE) Traffic Classes
  - APB or OCP for config
- Supports any data width
  - Typically 32 bits to 128 bits
- Mapping between interconnect Traffic Classes (BE, LL, SVC)
- Power management, Connection/ Disconnection, QoS, Clock Management, Rate Matching, etc…

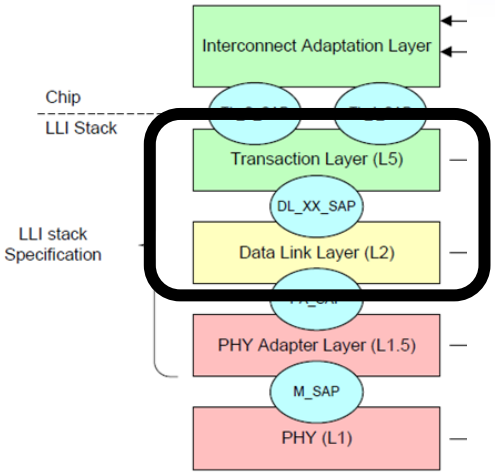


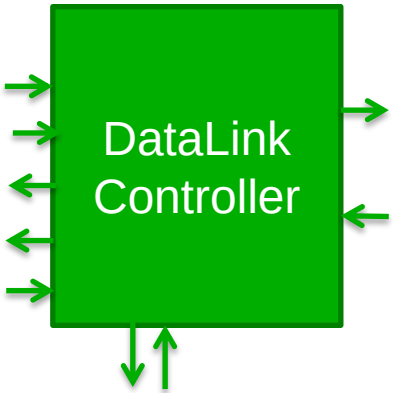




**Example Implementation*

# Transaction & Data Link Layers

- Example implementation embeds Transaction and Data Link Layers in DataLink Controller
- Usually same clock as interconnect
- Optional Master/Slave LL and BE TC ports
- Optional 40-bit LLI addressing
- Handles LLI clock conversions
- Performance parameters

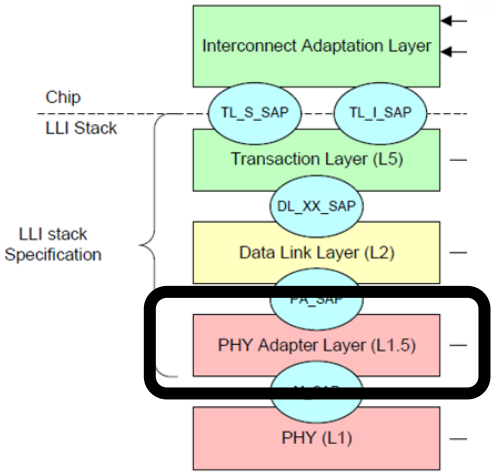


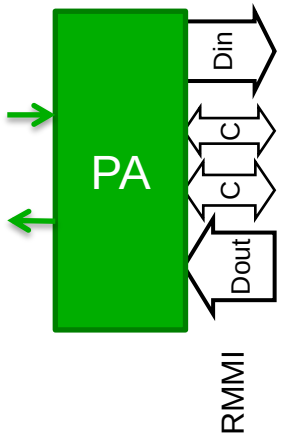




**Example Implementation*

# Physical Adapter Layer

- Interface to MIPI M-PHY
- Configurable number of Rx and Tx lanes
- Configurable RMMI data
- Optional PHY test mode

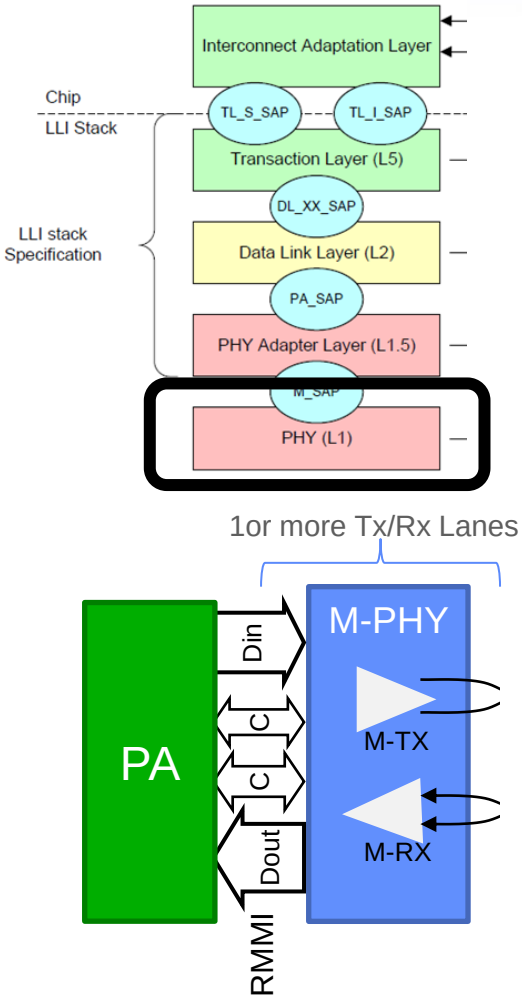



**Example Implementation*

# MIPI M-PHY

- Industry standard
- Optimized for mobile applications
  - High performance and scalability
  - Low power operation and modes
- LLI M-PHY features
  - Type 1
  - HS-Mode Gears G1, G2 or G3
  - Up to 5.8 Gbps per lane




**Example Implementation*

# Potential Future Developments

- Increased IPC Efficiency
  - Signaling, Low Latency, Memory Mapped Accessed, Memory Management
- Increased Link Efficiency
- Power Management Extensions

# Why MIPI LLI?

- Link a chip and a companion chip together
- Remove a memory chip from a mobile phone
- No software complexity
- Fewer pins than other standards
- Scalable – Future-proof designs for high-throughput requirements
- Low Power – Leverage M-PHY (< pwr than PCIe)

Increase Flexibility, Reduce BoM cost